Lab #6 Analog to Digital Convertor

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1. Objective

We aim to build an analog to digital convertor (ADC). The analog input to be used is a constant DC voltage. Using various circuit elements, such as logic gates, Op-Amps and flip flops, this input will be converted to a digital output and displayed using a counter.

2. Background

The circuit that we attempt to build in this lab is described in the image below:

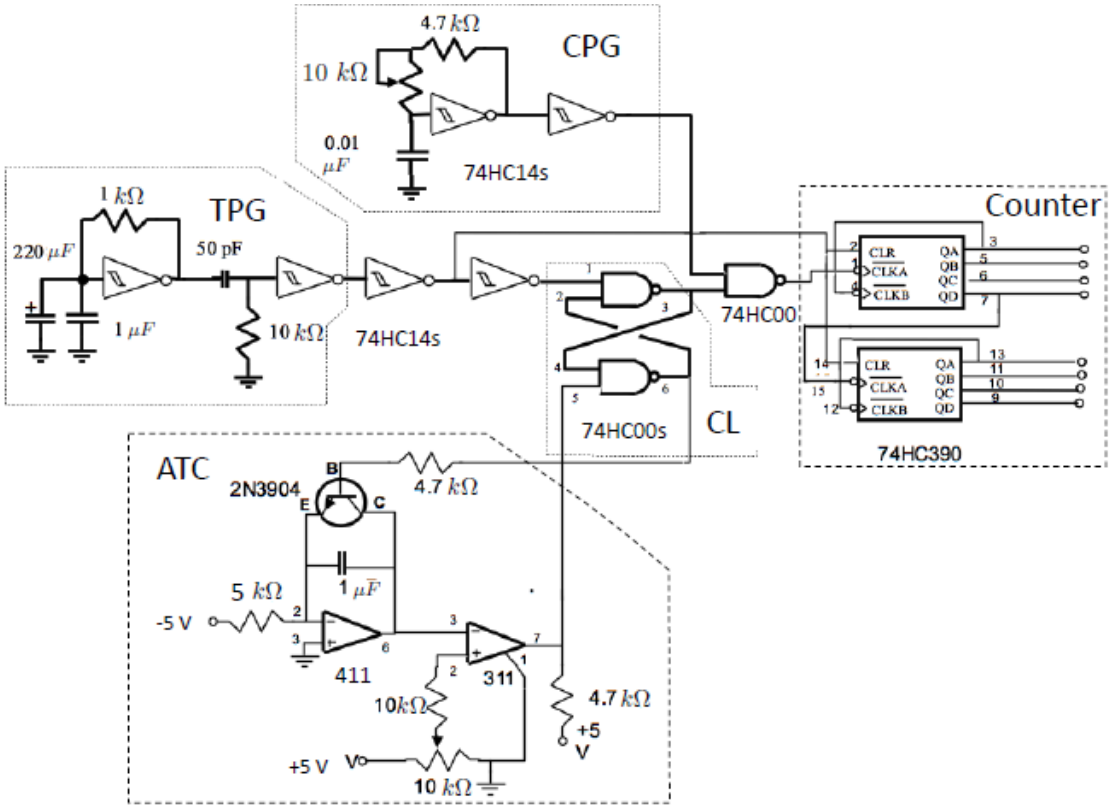

Figure: Final ADC Circuit

The CPG (Clock Pulse Generator) portion of the circuit above is responsible for creating a series of regular square pulses. The frequency of these pulses can be varied using the variable resistor.

The TPG (Trigger Pulse Generator) part of this circuit is responsible for for creating a trigger pulse when the counter is to be Reset. The output of this part of the circuit is constantly high except for a regular negative pulse.

The TPG and CPG both use Schmitt Triggers, which are know to have hysteresis as a feature. This allows them to switch from Low to Hi and Hi to Low at different voltage levels. The result of this feature is a noise resistant trigger.

The ATC (Analog to Time Converter) portion of the circuit allows us to convert the voltage provided as an input (our analog signal) to a time window by using OpAmps configured to work as an Integrator and Comparator.

The CL (Control Logic) allows for all of these signals to be processed and converted to digital outputs

The counter allows us to interface the digital signals with a 7 segment LED Display.

We continue to explore these sections of the circuit and develop our understanding of them in the sections below.

3. Experiment

3.1 Trigger Pulse Generator

3.1.1 Hysteresis of Schmitt-trigger

The Schmitt Trigger is a special type of trigger where the input voltage level to cause the output to transition between states depends on the output state of the inverter. In this section, we attempt to measure the levels at which the trigger switches states. To do so, we used the Schmitt Trigger chip.

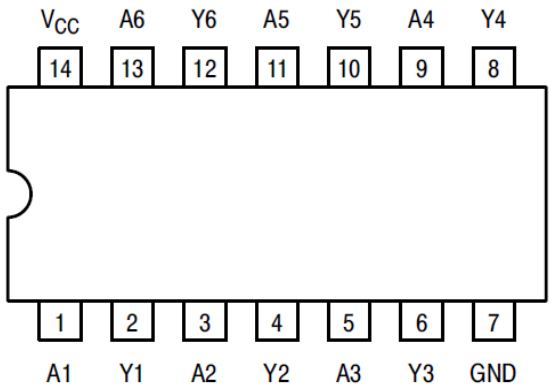

Figure 1: Schmitt Trigger Chip

Here, Inputs correspond to channel labels beginning with A, outputs correspond to channel lables beginning with Y, V_cc refers to the input voltage and GND refers to Ground Input.

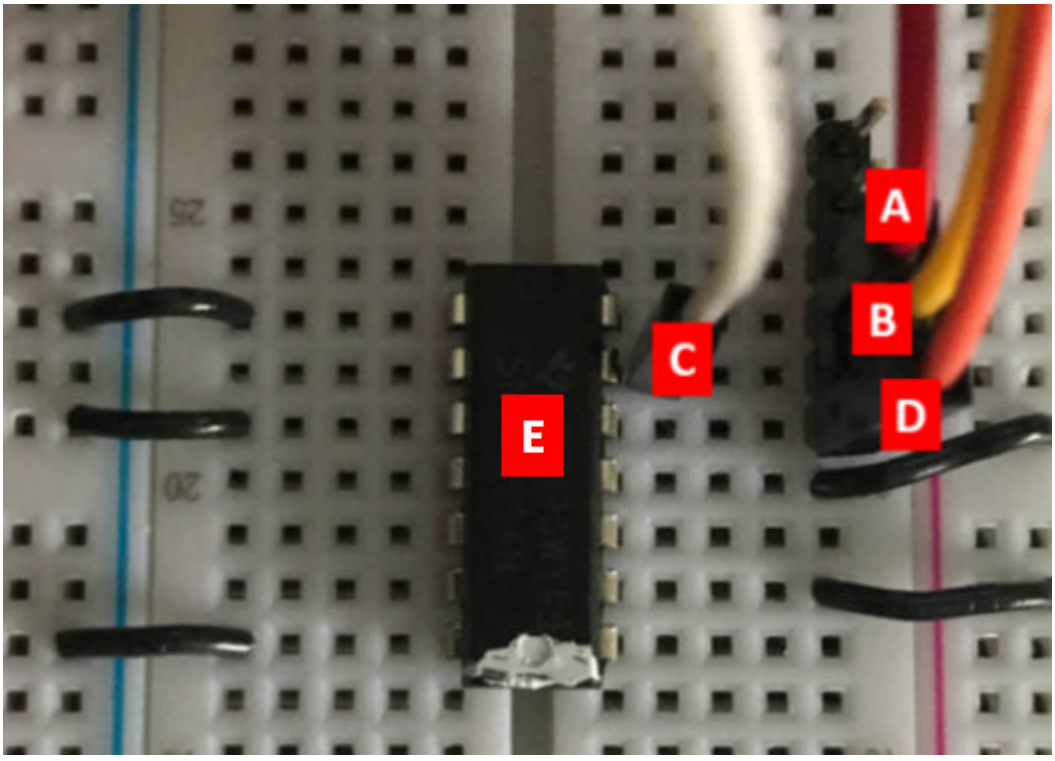

Figure 2: Assembled Experiment Cicuit

A: V_cc of 5V

B: Wave generator input

C: Oscillioscope Channel 2

D: Oscilloscope Channel 1

E: Schmitt Trigger Chip

In Figure 2, all inputs to the chip, except the trigger that we are using, are grounded.

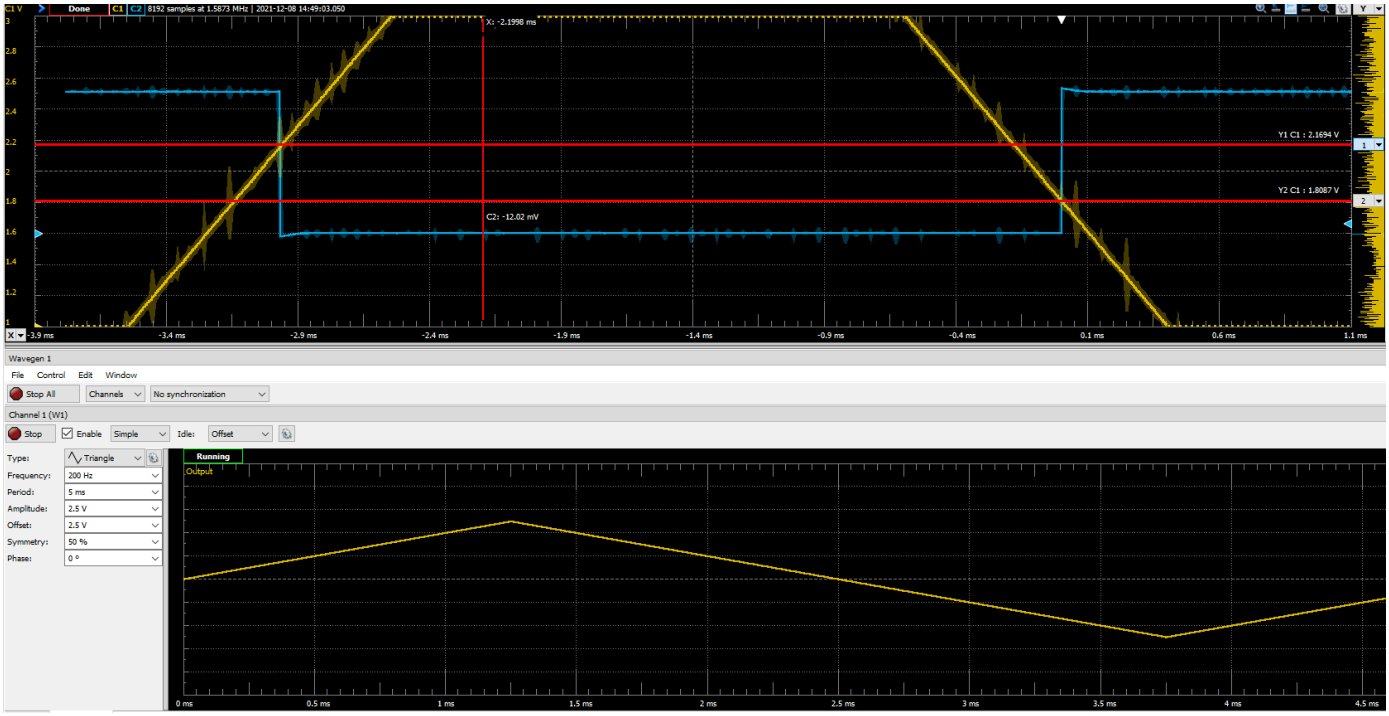

Figure 3: Oscilloscope Output vs Input for Schmitt Trigger. Blue corresponds to Output. Yellow Corresponds to Input

```
Hi_To_Lo_SwitchVoltage_V=[2.17];
Lo_To_Hi_SwitchVoltage_V=[1.8087];
Uncertainty_Lo_To_Hi_V=[0.2];
Uncertainty_Hi_To_Lo_V=[0.2];
table(Hi_To_Lo_SwitchVoltage_V,Uncertainty_Hi_To_Lo_V,Lo_To_Hi_SwitchVoltage_V,Uncertainty_Lo_T
```

```
ans = 1×4 table
```

...

	Hi_To_Lo_SwitchVoltage_V	Uncertainty_Hi_To_Lo_V	Lo_To_Hi_SwitchVoltage_V
1	2.1700	0.2000	1.8087

Uncertainty of these values (and all following cursor measurements from the oscilloscope) is based on the uncertainty caused by manual placement of cursors at measurement points. Since we are limited by the level of zoom possible, fuzziness of signal at high zoom and the thickness of the cursor, these compound to an approximated $\pm 0.2\ V$ uncertainty. Please note that the cursors were placed when mpore zoomed in and not at the zoom shown in the image above.

These experimental values are within the range of the values provided in the data sheet. In the datasheet for the Schmitt Trigger, for a V_cc input of 5V, the switching voltage for LO to HI is given in the range of 2.0-3.3 V while LO to HI is given in the range of 1.3-2V.

The feature of Schmitt triggers having different trigger Voltages depending on the output can be useful due to the noise immunity provided. In a trigger without this feature, a signal with significant noise would cause fluctuations between on and off state as the signal oscillates around a trigger level. On the other hand, with a Schmitt trigger, once triggered once, the signal would then have to reach the second trigger level, which is not very close to the first. This means signals would have to either have very significant noise where both trigger levels are acheived if the noise were to affect the circuit.

Additionally, when working with signals with long rise and fall times, the Schmitt trigger is suitable for converting this to an effectively digital signal, as the trigger will only trigger once during the rise and then once during the fall, switching from Lo to Hi and Hi to Lo resepctively

3.1.2 Square Wave Oscillator

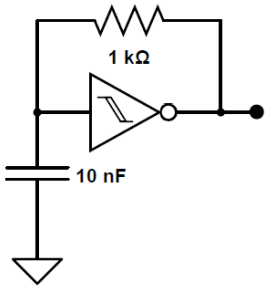

Figure 4: Circuit Diagram

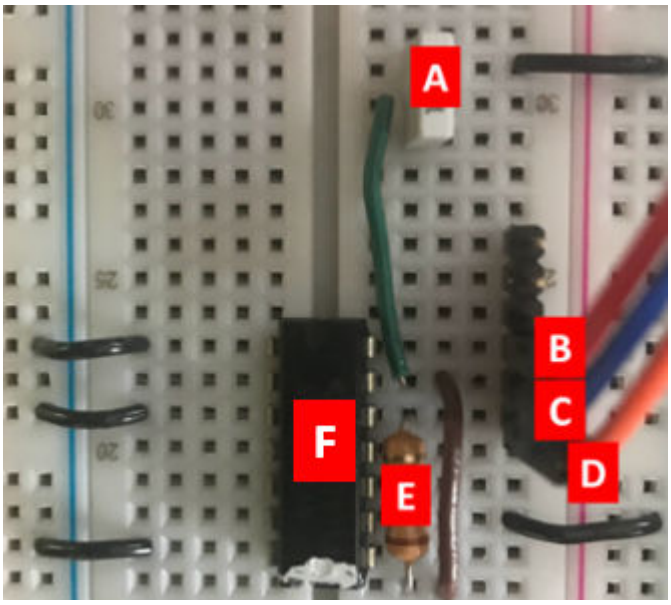

Figure 5: Constructed Square Wave Oscillator

A: $10.93\ \text{nF} \pm \frac{0.01}{\sqrt{3}}\ \text{nF}$ Capacitor

B: V_cc of 5V

C: Scope Channel 2

D: Scope Channel 1

E: $0.93\,\Omega \pm \frac{0.001}{\sqrt{3}}\,\Omega$ Resistor

F: Schmitt Trigger Chip

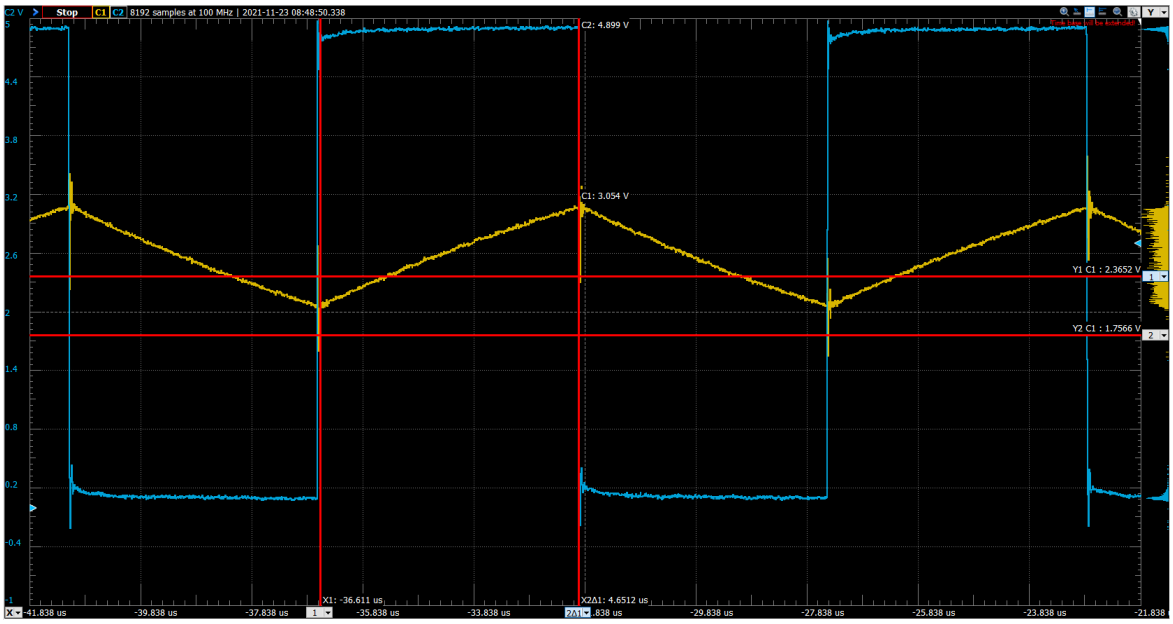

Figure 6: Scope Measurement

As capacitor charges and discharges, the schmitt trigger switches from on to off. The voltage at which the change occurs is within the range of uncertainty of the Hysteresis result from the previous section. The frequency of the oscillation is 107.5 kHz.

Calculation of Frequency:

$$f = \frac{1}{\Delta t} = \frac{1}{2 * (4.6512 * 10^{-6})} = 107.5\,\text{kHz}$$

Calculation of Uncertainty:

$$\left(\frac{\Delta t_1}{t_1} + \frac{\Delta t_2}{t_2}\right) * f = \Delta f = \pm 3\,\text{kHz}$$

The uncertainties of the 2 times used was based on the uncertainty in the manual placement of cursors. Cursors were placed with much more zoomed in scope displays than waht is used above.

3.1.3 Short Pulse Rectifier

The short pulse rectifier is constructed by connecting the output of the circuit above to the following circuit.

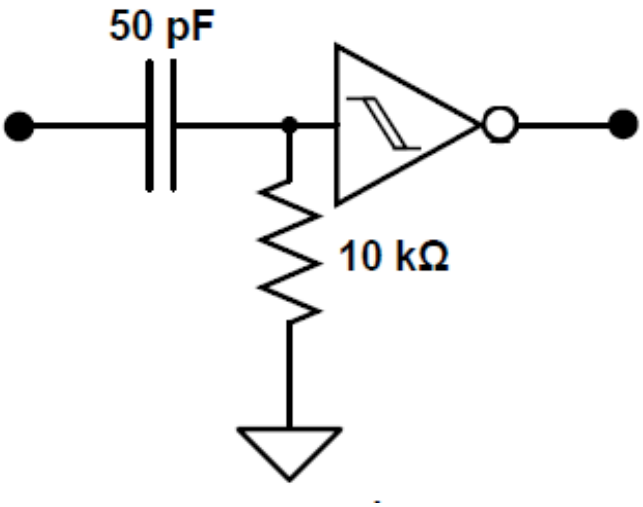

Figure 7: Short Pulse Rectifier

In this circuit, the output of the the circuit from 3.1.2 is taken as an input. With this circuit, we consider the small capacitance of the 50 pF capacitor, relative to the 10 nF capacitor in the previous circuit. As a result of this, this part of the circuit will have a much smaller time constant, meaning during the square wave output of the first circuit, the capacitor charges and discharges very quickly. When the square wave output of the first circuit is high, the capacitor is discharged and acts a short to the second Schmitt trigger, this allows the output to swtich to LO as the voltage input exceed the required level (5V> 2.17V). As the capacitor charges up, this voltage input reduces until a point where it is equivalent to the LO to HI trigger voltage and the output of the 2nd trigger will once again be HI. This is maintained until the capacitor is charge completely, at which point the capacitor acts as an open circuit, resulting in no connection from the HI output of the square wave, and ground is seen by the input of the 2nd Schmitt Trigger. Once the output of the first trigger switches to 0 once again, the capacitor begins to discharges rapidly, meaning the input of the 2nd trigger remains at 0 or below 0, depending on what stage of discharge the capacitor is at. Once the output switches to HI again, the cycle repeats, and we get our short pulse, until our 50 pf capacitor is sufficiently charged.

We can calculate the expected width of the pulse using the formula:

$V_c = V_0 - V_0 e^{-\frac{t}{RC}}$ and $5 - V_c = V_{T-} = 1.8087$ This is the switching voltage that we found in a previous section

$t = -\mathrm{RC}\ln\left(\frac{(1.8087)}{5}\right)$

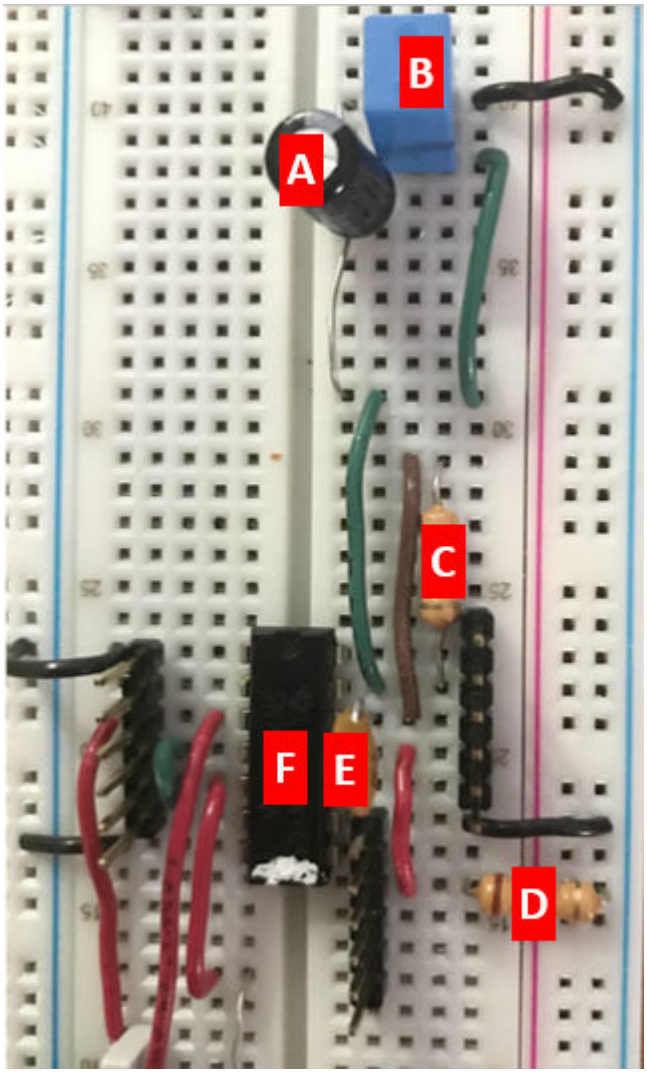

Figure 8: Assembled Short Pulse Rectifier

A: 221.3 $\pm\frac{0.1}{\sqrt{3}}\mu$F Capacitor

B: 1.035 $\pm\frac{0.001}{\sqrt{3}}\mu$F Capacitor

C: 1.02 $\pm\frac{0.01}{\sqrt{3}}$ kΩ Resistor

D:9.87$\pm\frac{0.01}{\sqrt{3}}$ kΩ Resistor

E: 47.3 $\pm\frac{0.1}{\sqrt{3}}$pf Capacitor

F: Schmitt Trigger Chip

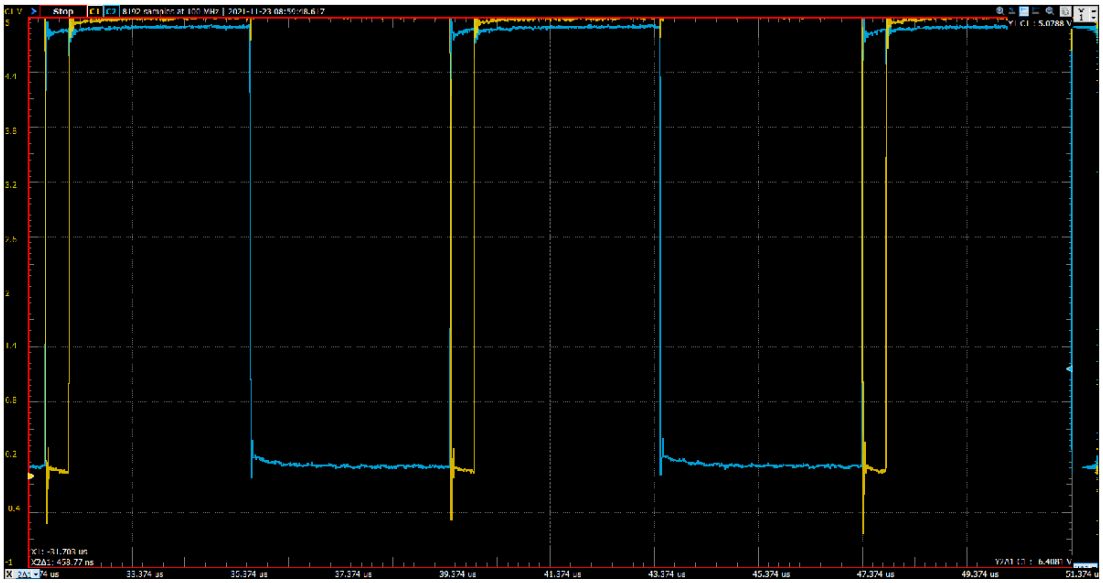

Figure 9: Experimental Output with 10 nF Capacitor in the square wave generator

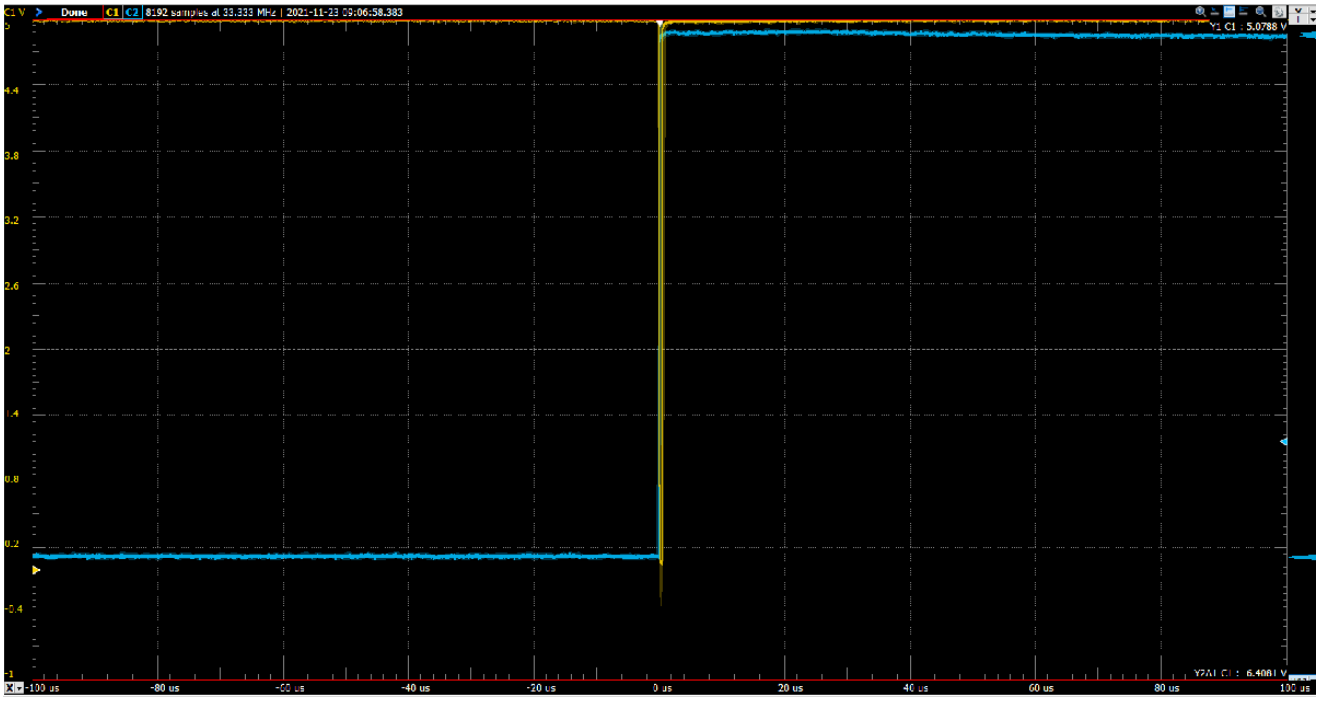

Figure 10: 221 μF for the square wave generator , resulting in the following pulse

With the increased capacitanc in the square wave generator portion of this circuit, the width of the each square pulse to the input of our circuit increases, resulting in a relatively narrower peak. This is because the high capacitance in the square wave generator results in a reduced pulse frequency.This should not affect the width of the trigger pulse, as all features of this section of the circuit remain the same (i.e. same resistance and capacitance be), meaning identical pulse width is expected. When measuring the pulse width with both capacitances, we get $624\text{ns} \pm 5\text{ ns}$.

Theoretical Square Pulse Width:

$$t = -\mathrm{RC}\ln\left(\frac{(1.808)}{5}\right)$$

$$t = 582.9\ \mathrm{ns}$$

Uncertainty:

$$\Delta t = \sqrt{\left(\frac{\partial t}{\partial R}\delta R\right)^2 \quad \left(\frac{\partial t}{\partial C}\delta C\right)^2 + \left(\frac{\partial t}{\partial V_{T-}}\delta V_{T-}\right)^2}$$

$$\Delta t = 35.3\ \mathrm{ns}$$

The actual pulse width is slightly higher than our theoretical width, even when accounting for our uncertainty. one observation from the experiment is that the switching voltage was slightly different with the capacitor and resisor than when we tested with the triangular input. As a result, the theoretical calculation may need to use this value rather than the switching voltage found in the first section. However, there is only a minor difference in the 2 values.

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We also attempt a theoretical calculation of the expected frequency of the square wave oscillator of this circuit.

Theoretical Calculation

Charging Capacitor time:

$$t_2 - t_1 = -\mathrm{RC} * \ln\left(\frac{(V_{t-} - V_{\mathrm{cc}})}{V_{\mathrm{cc}}}\right) \quad - -\mathrm{RC} * \ln\left(\frac{(V_{t+} - V_{\mathrm{cc}})}{V_{\mathrm{cc}}}\right) \quad = 0.085$$

Capacitor Discharge Time:

$$t_2 - t_1 = -\mathrm{RC} * \ln\left(\frac{(V_{t+})}{V_{\mathrm{cc}}}\right) - -\mathrm{RC} * \ln\left(\frac{(V_{t-})}{V_{\mathrm{cc}}}\right) = 0.090$$

$$f = \frac{1}{(\text{Charging Capacitor Time} + \text{Discharging Capacitor Time}) * 2)} = 5.67\ \mathrm{Hz}$$

Uncertainty

$$\Delta f = \sqrt{\left(\frac{\partial t}{\partial R}\delta R\right)^2 + \left(\frac{\partial t}{\partial C}\delta C\right)^2 + \left(\frac{\partial t}{\partial V_{T-}}\delta V_{T-}\right)^2 + \left(\frac{\partial t}{\partial V_{\mathrm{Tf}}}\delta V_{T+}\right)^2} = 5.3\ \mathrm{Hz}$$

Actual Value:

5.78 ± 0.04 Hz

The calculated frequency matches the experimental frequency within the range of it's uncertainty. We can use a similar method to calculate all theoretical frequencies for square wave. From this calculation, we can also conclude that increasing capacitance and resistance will both decrease the frequency of the final square wave, due to the linear proportionality to these factors in the calculation for frequency.

3.2 Clock Pulse Generator

In this circuit, we use a capacitor and potentiometer to create a square wave output that we can vary with time. The circuit is constructed as per the following diagram:

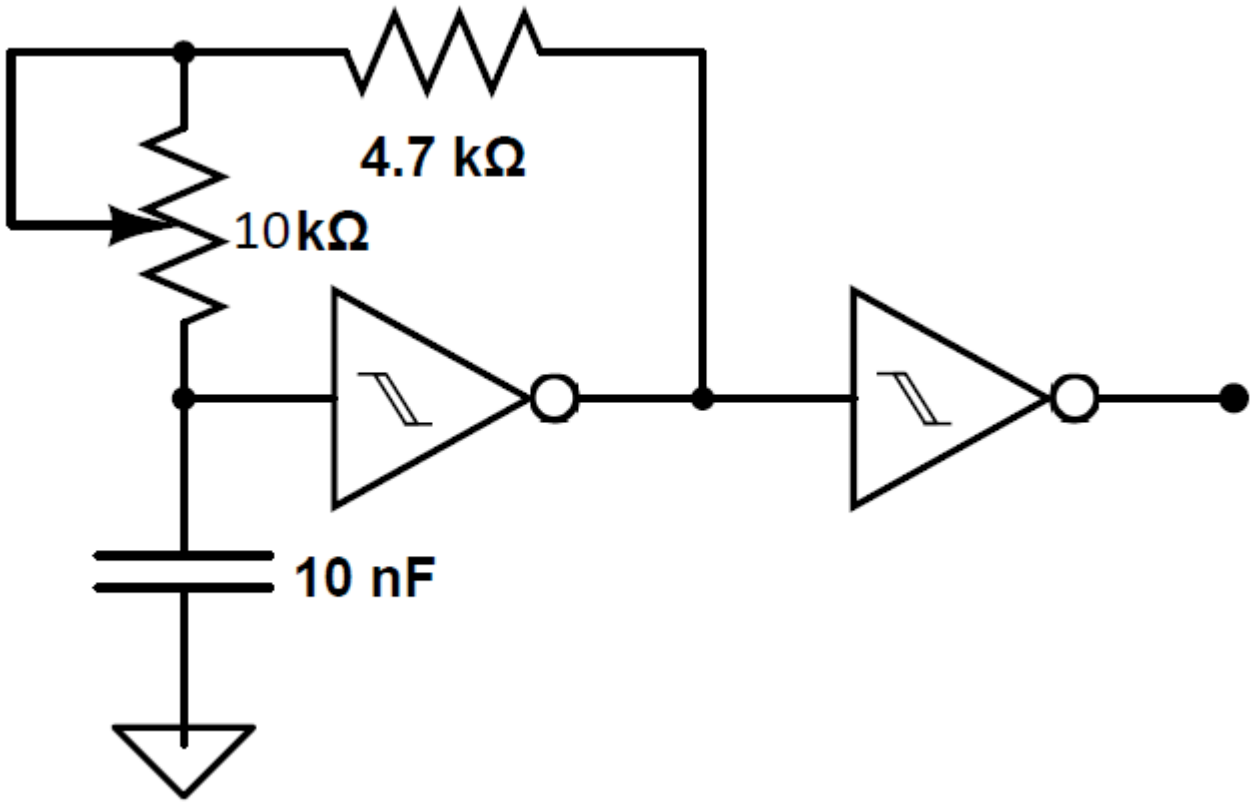


Figure 11: Circuit Diagram for Clock Pulse Generator

In the circuit above, the capacitor is able to charge up using the output of the first schmitt trigger. Once the voltage across the capacitor increases to a level corresponding to the voltage at which the trigger is triggered, the output voltage of the trigger drops to 0. This results in the capacitor discharging, and once it is discharged to a voltage level where the schmitt trigger would switch again, the trigger output switches to HI. Then, this cycle repeats with the capacitor recharging and discharging. This would result in an almost triangular input for the second Schmitt trigger, similar to the input during section 3.1.1, with the exponential charging and discharging of a capacitor resulting in this shape. As a result, we get a similar square pulse output from the second Schmitt trigger. The frequency of the square pulse would depend on the speed at which the capacitor recharges and discharges. This is dependent on the time constant of the capacitor, given by $R * C$, as the discharging of a capacitor is described by $V_c = V_0 e^{-\frac{t}{RC}}$. Therefore, by increasing resistance or capacitance, we expect a slower pulse frequency.

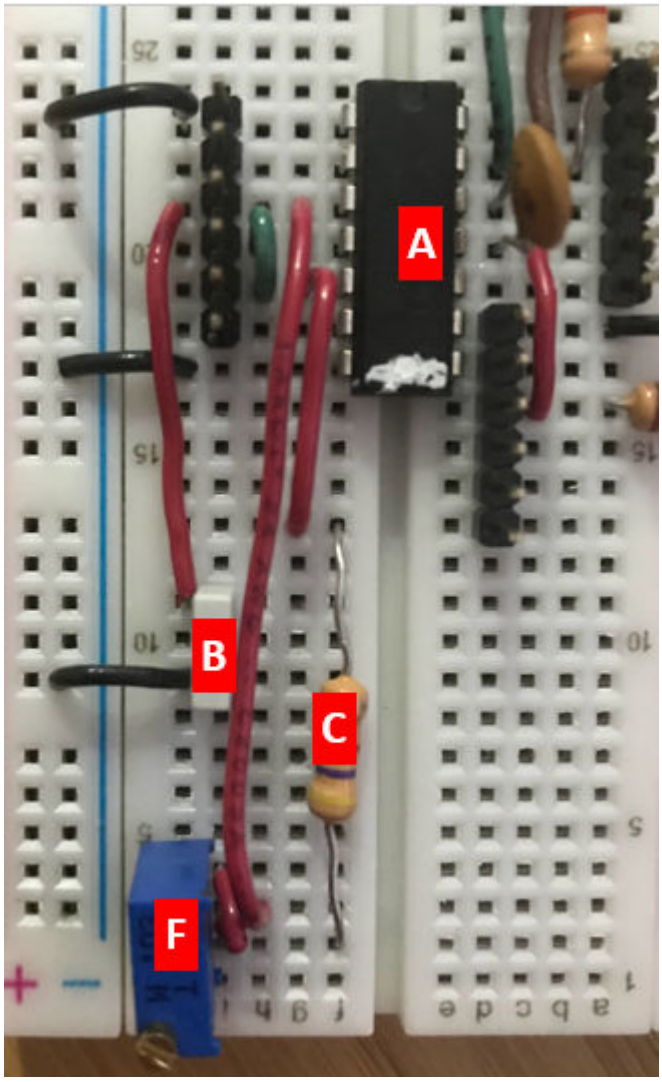


Figure 12: Constructed Clock Pulse Generator

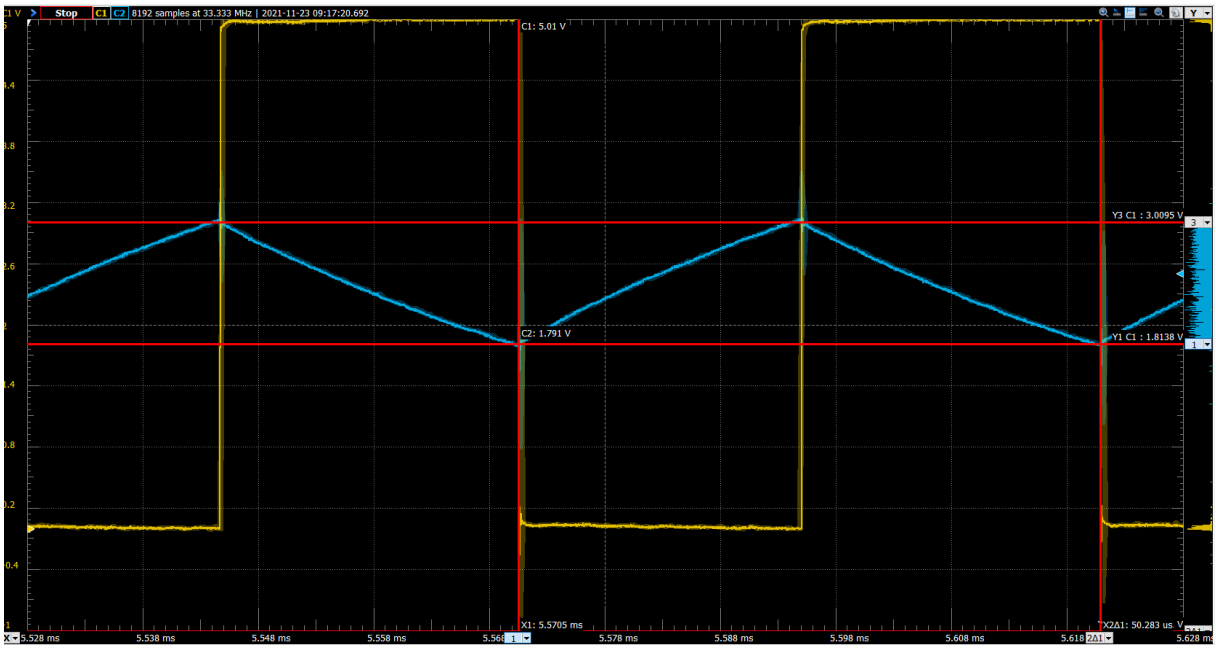
A: Schmitt Trigger Chip

B: 10.03 $\pm\frac{0.01}{\sqrt{3}}$nF Capacitor

C: 4.7 $k\Omega$ Resistor

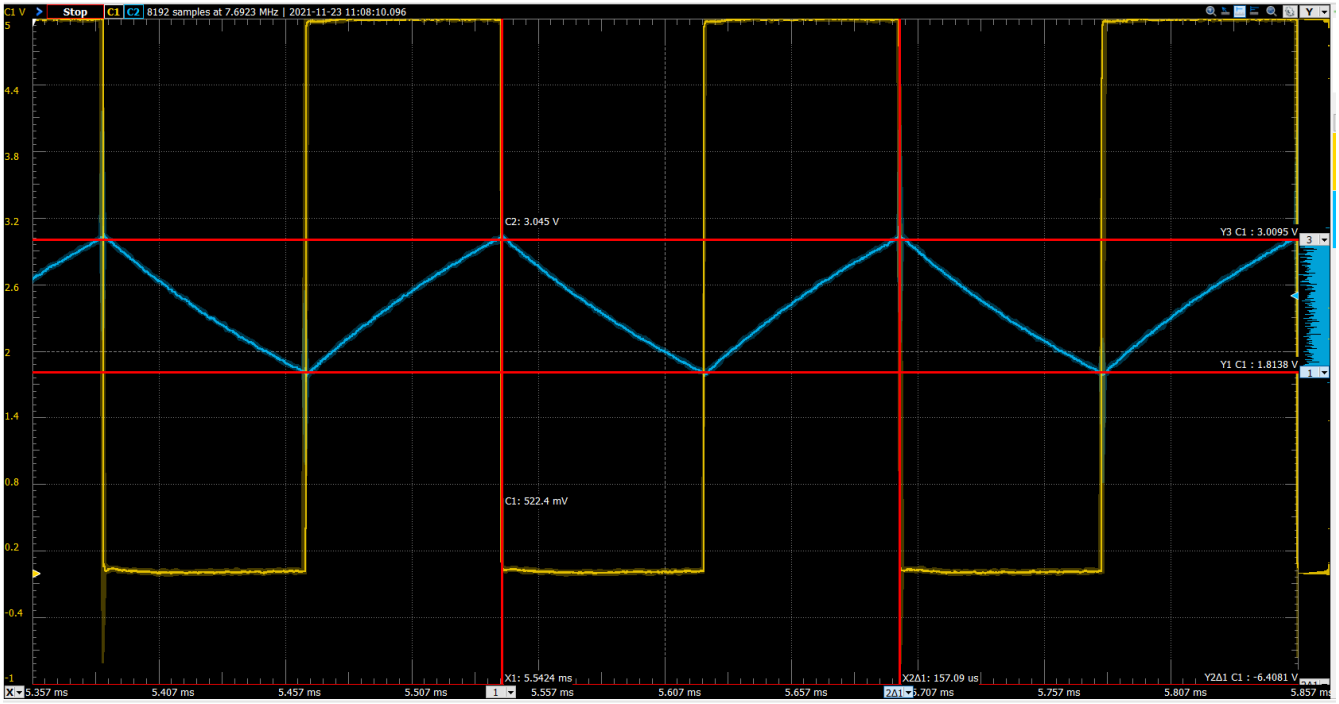
F: 10.3 kΩ Potentiometer

Figure 13: Clock Pulse Generator Output with 0 resistance from the Poentiometer



In Figure 13, the yellow line shows the output of the clock pulse generator while the blue line (channel 2) shows the input. We can see the almost triangular behaviour of the input due to the capacitor's charge/discharge cycle. With 0 resistance from the potentiometer, we see the highest possible pulse frequency with the circuit setup above, and the square wave generated has a pulse frequency of 19.9 $\mathrm{kHz} \pm 1.3\,\mathrm{kHz}$.

Figure 14: Lower Frequency Clock Pulse, with maximum resistance from the Potentiometer



Here, the yellow line (channel 1) shows the output of the clock pulse generator while the blue line (channel 2) shows the input. This has a pulse frequency of 6.4 $\mathrm{kHz} \pm 1.3\,\mathrm{kHz}$

Uncertainties and measurements were taken as seen in previous sections

As we have calculated expected square wave frequency in the previous section, I do not redo it here. As we can see from this section, we are able to create a square wave generator that can be varied with the potentiometer in a range of 6.4 kHz to 19.9 kHz.

3.3 Counter

In this section, we use a counter chip and combine 2 decade counters together to get a $\div 100$ counter. The counter chip is as seen in the diagram below:

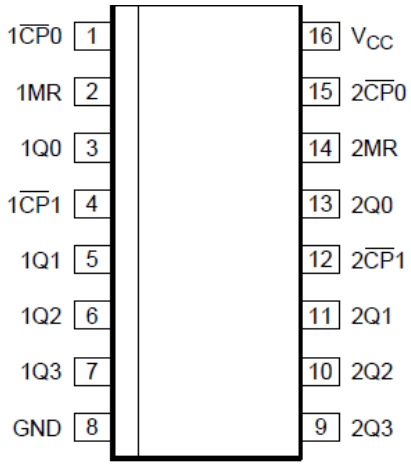


Figure 15: Counter Chip

Symbol	Pin	Description
1$\overline{CP}$0, 2$\overline{CP}$0	1, 15	clock input divide-by-2 section (HIGH-to-LOW; edge-triggered)
1MR, 2MR	2, 14	asynchronous master reset input (active HIGH)
1Q0, 1Q1, 1Q2, 1Q3	3, 5, 6, 7	flip-flop outputs
1$\overline{CP}$1, 2$\overline{CP}$1	4, 12	clock input divide-by-5 section (HIGH-to-LOW; edge-triggered)
GND	8	ground (0 V)
2Q0, 2Q1, 2Q2, 2Q3	13, 11, 10, 9	flip-flop outputs
V_{CC}	16	supply voltage

Figure 16: Counter Chip Symbol Descriptions

The $\div 2$ counter is able to output either a 0 or a 1 from the 1Q0 channel in the diagram above, with a high to low transition input to the tCP0 (clock input). The 1MR and 2MR pins seen above act as reset switches, when they are HIGH, the counter is reset to a 0 state. In order to test the $\div 2$ functionality, we ground the reset and input the following to the 1CP_0 channel (input for $\div 2$ counter). using the patterns app and logic analyzer. Using patterns (lower left section of screenshot), we input a pulse with 2 Hz frequency. We see the resultant output, labelled Q1 in the logic analyzer (top section of screenshot) and how this lines up with the input. As we can see, as the input goes from HI to LO, the Q1 output of the $\div 2$ counter changes states.

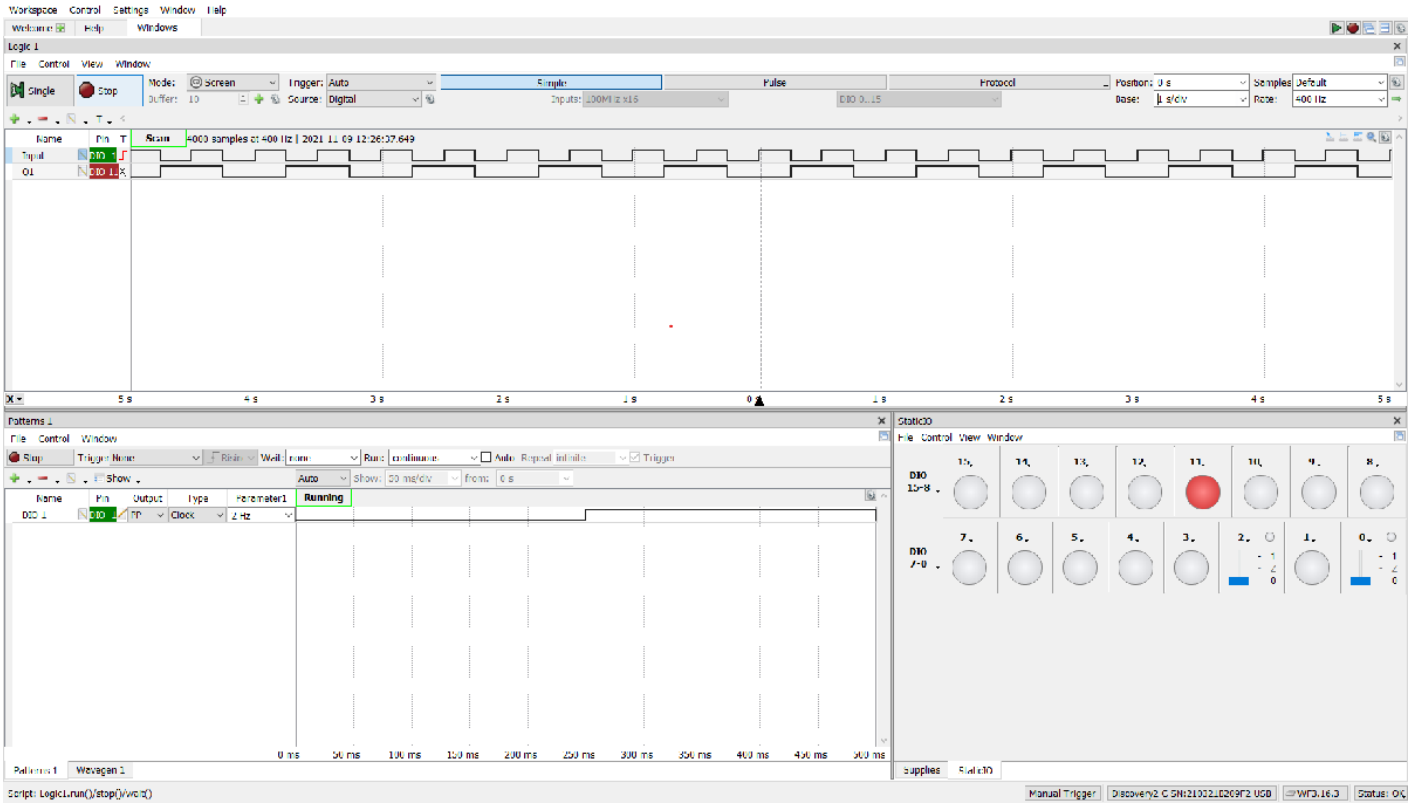


Figure 17: $\div 2$ Counter Testing with Logic Analyzer and Patterns.

When we then connect this to the output of this counter to the input of our $\div 5$ counter ($\mathrm{Q0\ to\ 1CP1}$), we expect to get a $\div 10$ counter. When these are connected, each time the output of the $\div 2$ counter switches from HI to LO, the $\div 5$ counter increments by 1. This results in outputs as seen in the table below for Q1, Q2, Q3 and Q4. We can convert this to an integer number by representing Q0, Q1, Q2 and Q3 by $2^0, 2^1, 2^2$ and 2^3 resepectively:

```
Q0=[0;1;0;1;0;1;0;1;0;1];
Q1=[0;0;1;1;0;0;1;1;0;0];
Q2=[0;0;0;0;1;1;1;1;0;0];
Q3=[0;0;0;0;0;0;0;0;1;1];
IntegerVal=[0;1;2;3;4;5;6;7;8;9];
table(Q0,Q1,Q2,Q3,IntegerVal)
```

```
ans = 10×5 table
```

	Q0	Q1	Q2	Q3	IntegerVal
1	0	0	0	0	0
2	1	0	0	0	1
3	0	1	0	0	2
4	1	1	0	0	3
5	0	0	1	0	4
6	1	0	1	0	5
7	0	1	1	0	6

	Q0	Q1	Q2	Q3	IntegerVal
8	1	1	1	0	7
9	0	0	0	1	8
10	1	0	0	1	9

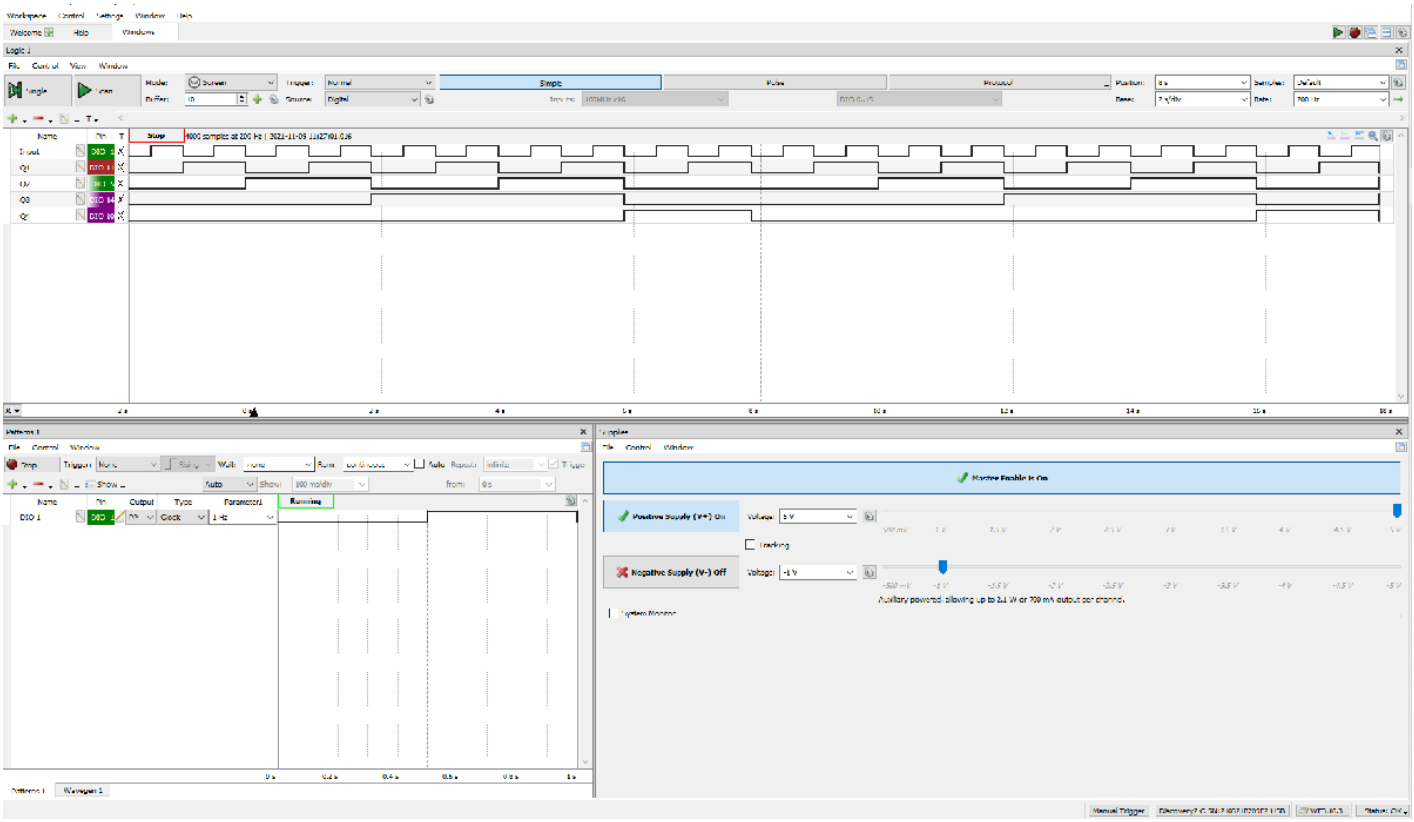


Figure 18: $\div 5$ counter testing using Logic Analyzer and Patterns

We see this circuit outputting the values expected from the table above in the logic analyzer from the image above (top part of screenshot). All channels are labelled to match their relevant table columns and an input to the first $\div 2$ counter of a clock pulse is seen in the bottom left of the window. This allows the counter to incremeent.

Connecting the ouput of Q3 of this $\div 5$ counter to the input another $\div 10$ counter allows us to achieve a $\div 100$ counter, as each time we pass integer 9 on our first counter, the ouput to the 2nd counter will go from HI to LO, incrementing the 2nd counter by 1. We verify this function by constructing the following circuit:

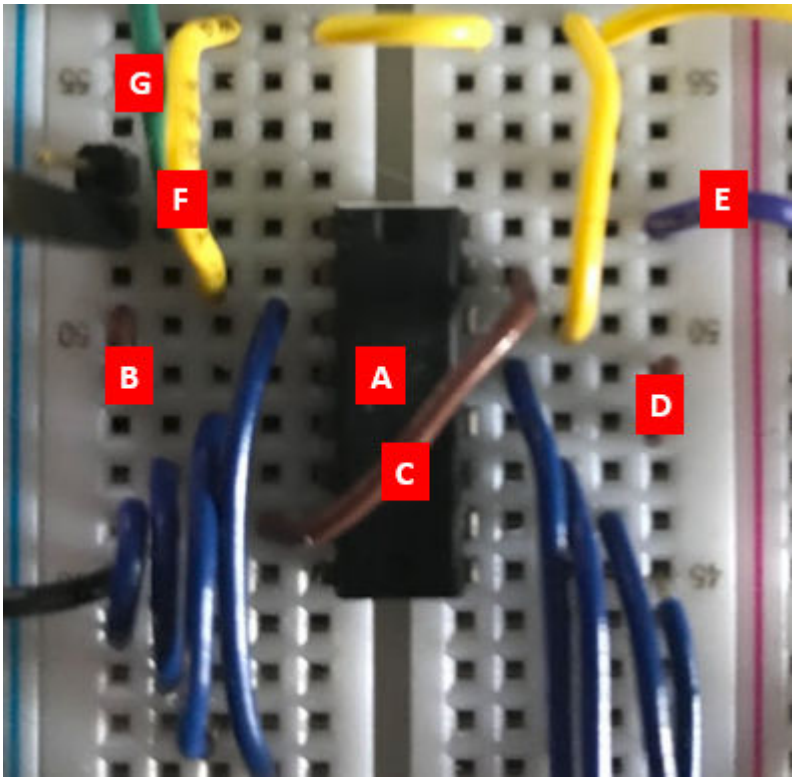


Figure 19: Constructed $\div 100$ counter

A: Counter Chip

B: Connection between Q0 and Input for $\div 5$ counter

C: Connection between Q3 and 2nd $\div 2$ counter

D: Connection between Q0 of the 2nd $\div 2$ counter and Input for the 2nd $\div 5$ counter

E: Voltage Supply

F: Ground for Reset switches

G: Pulse Input

The video linked below shows the outputs of the counter connected to an LED 7 segment display, with the first $\div 10$ counter connected to the first digit, and the second to the second digit. We input a pulse from our wavegenerator, initially at 1 Hz, and the counter counts up by 1 digit per second since we have 1 HI to LO transition per second. By doing so, we can verify that out $\div 100$ counter is working as expected. We can also see that increasing the frequency in the wavegen results in an increased speed of counting in the video. Additionally, I tested to see that a LO to HI pulse will reset the counter. Unfortunately one segement of the 7 segment display was not functioning during this experiment, but observations can still be made taking this into account.

https://youtu.be/ZAflo-FDJd4

3.4 Analog to Time Converter

3.4.1: Integrator

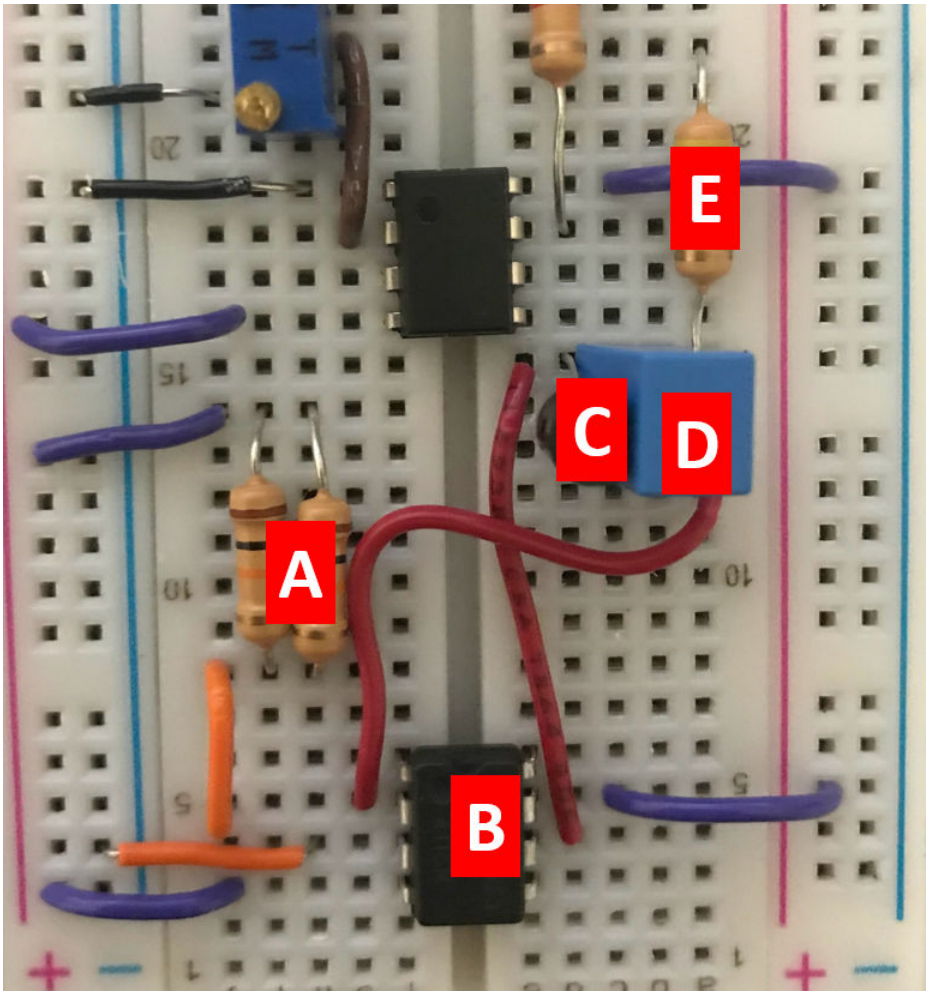


Figure 20: Constructed Integrator Circuit

A: 2 $10\,k\Omega$ Resistors in parallel to form a 5 $k\Omega$ resistor

B: 411 Comparator OpAmp Chip

C: Transistor

D: Capacitor

E: $4.7\,k\Omega$ Resistor

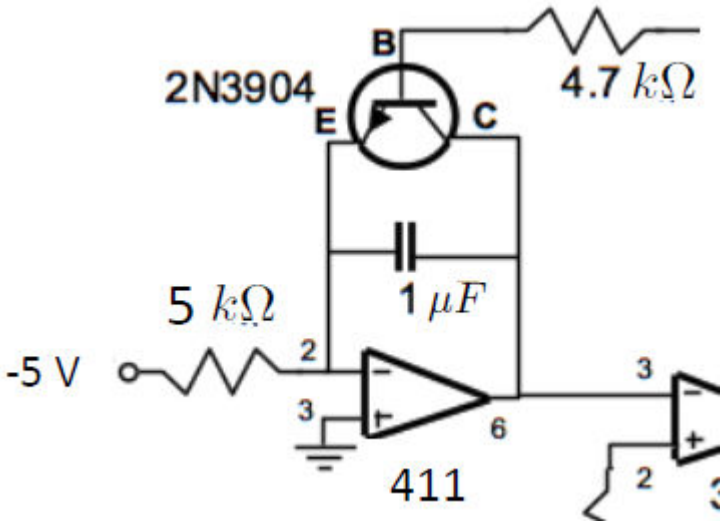


Figure 21: Integrator Circuit Diagram

The circuit above uses an OpAmp in the integrator configuration to generate a voltage ramp. This circuit is controlled by an input current through the 4.7 kΩ resistor in the drawing above. When the voltage is HI, the transistor results in a short across the capacitor. Since we know the Voltage at the point labelled 2 is 0, based on the rules of OpAmps having equal voltage at both input terminals, the output voltage will also be 0. When the input voltage to the 4.7 kΩ resistor is instead LO, the capacitor connects point 2 and 6 in the circuit above. From here, we can analyze the circuit using the rules of OpAmps. As we know that the voltage at 2 must be 0 and no current can flow into the OpAmp, we can equate the current through the 5 kΩ resistor to the capacitor by the following:

$$\frac{V_2 - V_{\text{in}}}{5\ k\Omega} = I_{\text{in}} = I_{\text{out}} = C\ \frac{\text{dV}_c}{\text{dt}}$$

Here, V_2 is 0 as we know from the rules of OpAmps, and V_c will be equal to the output voltage. We then rearrange to get the following:

$$-\frac{V_{\text{in}}}{5k\Omega * C} = \frac{\text{dV}_c}{\text{dt}} \rightarrow V_c = -\int \frac{V_{\text{in}}}{5\ k\Omega * C}\text{dt} = -\frac{V_{\text{in}} * t}{5k\Omega * C}$$

As a result, we can expect a stright diagonal line with slope of $\frac{-V_{\text{in}}}{5\ k\Omega * C}$ as the output of this circuit when the input to the transistor is Lo.

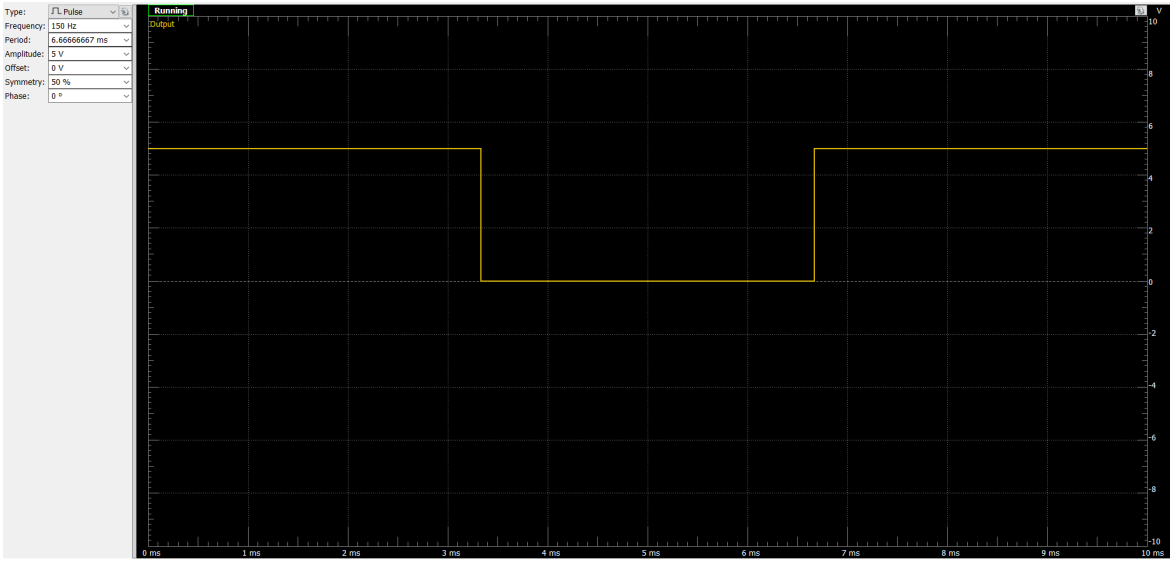


Figure 22: Pulse Input to 4.7 kΩ resistor

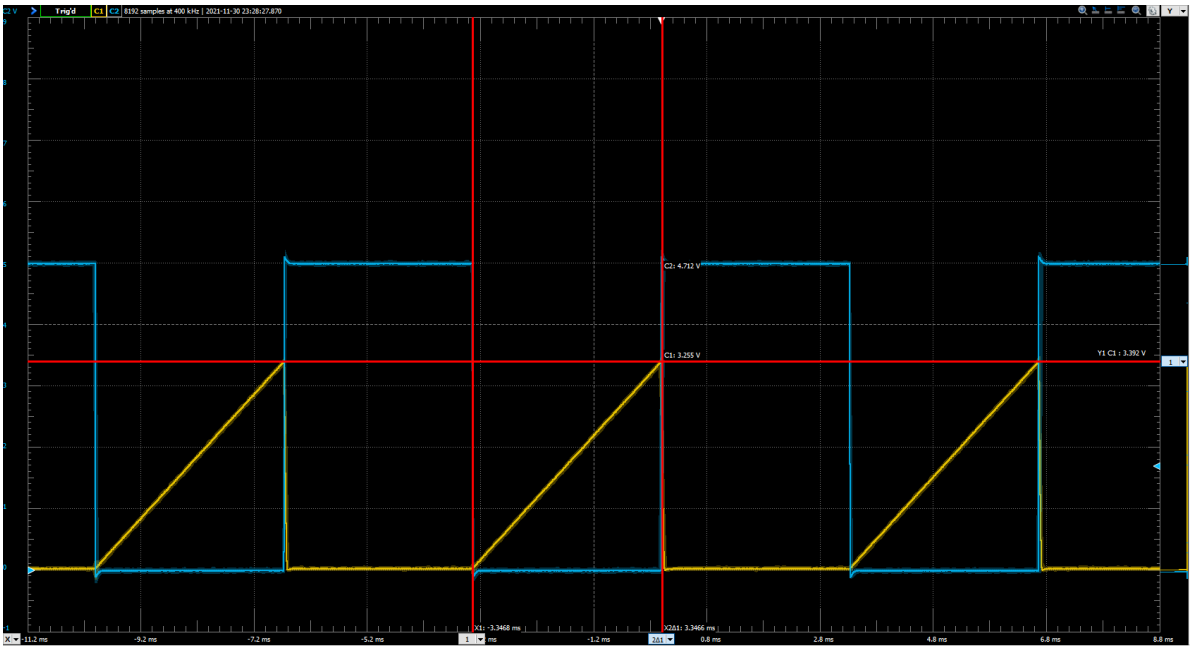


Figure 23: Scope Output, Yellow Line (channel 1) shows output of OpAmp, Blue Line (channel 2) shows pulse input to Resistor

As we can see above, the circuit functions as expected, with a diagonal line as the capacitor charges up when the transistor has a LO input. We also see a LO output of 0V when the transistor has a HI input, as the capacitor is shorted. We compare the slope of the ramp to what is expected by our derivation above.

Expected Slope:

$$\frac{V_{\text{in}}}{4.97\,k\Omega * C} = \frac{5}{4.97 * 0.98 * 10^{-3}} = 1000\,\frac{V}{\Omega F}$$

Actual Slope:

$$\frac{V_2 - V_1}{T_2 - T_1} = \frac{3.255}{3.346 * 10^{-3}} = 972 \ \frac{V}{\Omega F}$$

Uncertainty in Expected Value:

$$\left(\frac{\delta V}{V_{\text{in}}} + \frac{\delta R}{R} + \frac{\delta C}{C}\right) * \text{slope} = \pm 79 \ \frac{V}{\Omega F}$$

Uncertainty in Experimental Slope

$$\left(\frac{\delta V_2 + \delta V_1}{V_2 - V_1} + \frac{\delta T_2 + \delta T_1}{T_2 - T_1}\right) * \text{slope} = \pm 165 \ \frac{V}{\Omega F}$$

As can be seen by our calculations, the theoretical slope is within the range of uncertainty from our measured slope. We observe the behaviour of our OpAmp to create a voltage ramp when the input at the resistor connecting to the base of our transistor is low. We also notice that there is a saturation voltage, past which the integrator is unable to continue increasing the voltage ramp. In the oscilloscope screenshot below, we can see that this occurs at $4.21 \pm 0.04V$ This is due to the limited supply voltage of 5 V available to the OpAmp, and loses within the chip preventing the OpAmp from acheiving this full voltage.

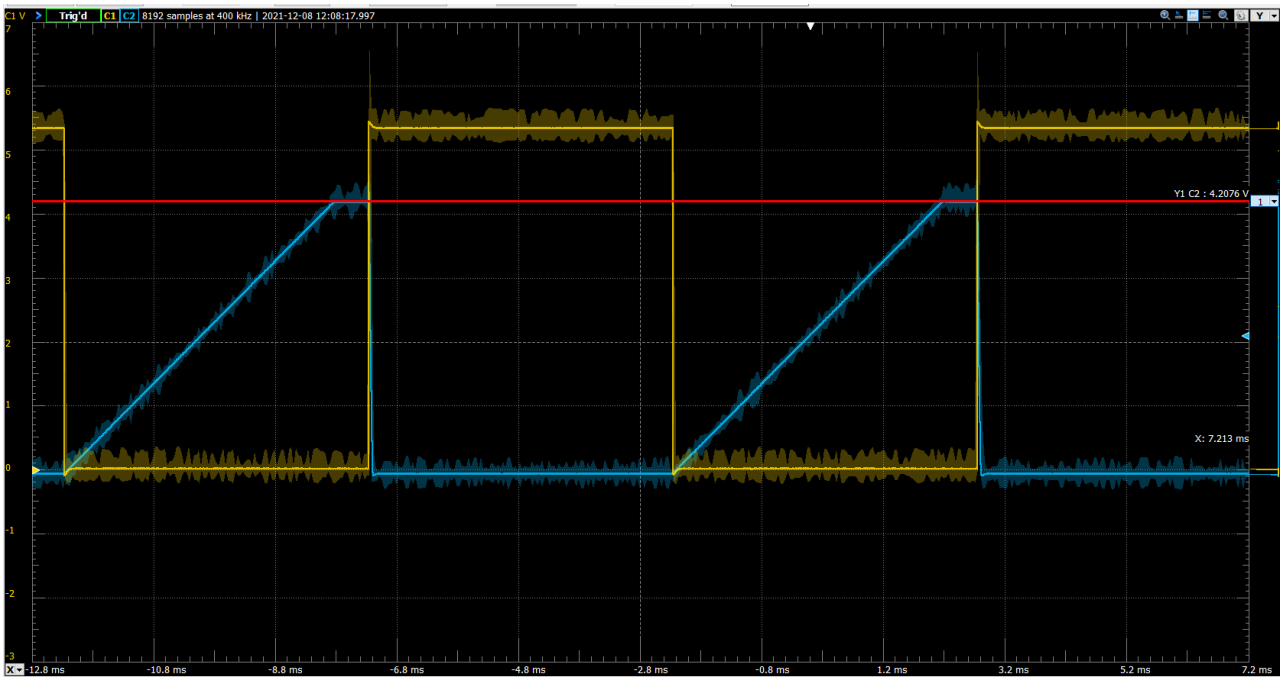


Figure 24: Integrator Circuit Output (Blue Channel 2) and Input (Yellow Channel 1)

As we vary frequency across the range at which the OpAmp is still able to integrate, we do not observe a change in the slope of the ramp (see image below), which is as expected based on our calculations above.

We could further test our calculations by attempting to vary the resistance or capcitance used and observing whether the resultant slope change can be described by the expected slop equation above.

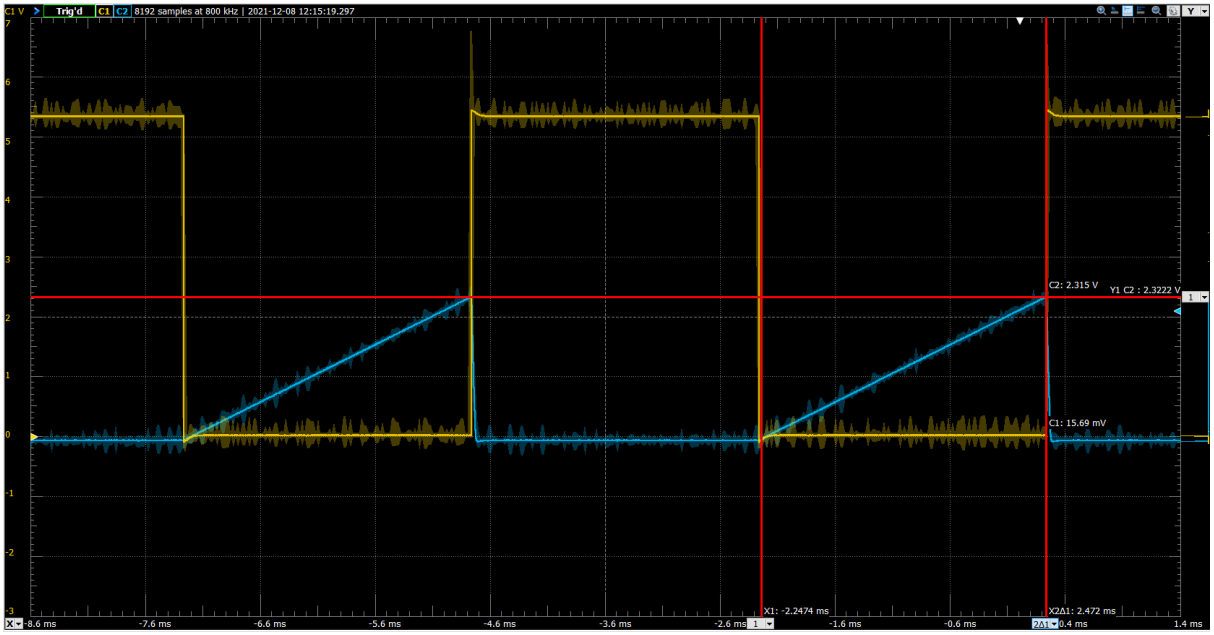


Figure 25: Lower frequency yet same slope for the integrator (calculated to be: 936.5 ± 93)

So, we can use this circuit to create a voltage ramp, whose maximum voltage achieved can be varied by changing the frequency of the input square pulse voltage. The maximum voltage achieve is limited to $4.2 \pm V$ due to the limited supply voltage of the OpAmp. This OpAmp is rated up to supply voltage 18V based on the data sheet, so we expect to be able to achieve a ramp closer to 18V with sucha a supply voltage, bu this was not tested due to fear of blowing the chip.

3.4.2: Comparator

The second part of this section focuses on using the output of our previous section with a comparator. The comparator works to compare the voltage provided at the positive input to the voltage at the negative input. While the voltage at the positive input is exceeded or matched by the input of the negative terminal, the OpAmp outputs Lo. At all the other times, the output is expected to be Hi. The constructed circuit is seen below:

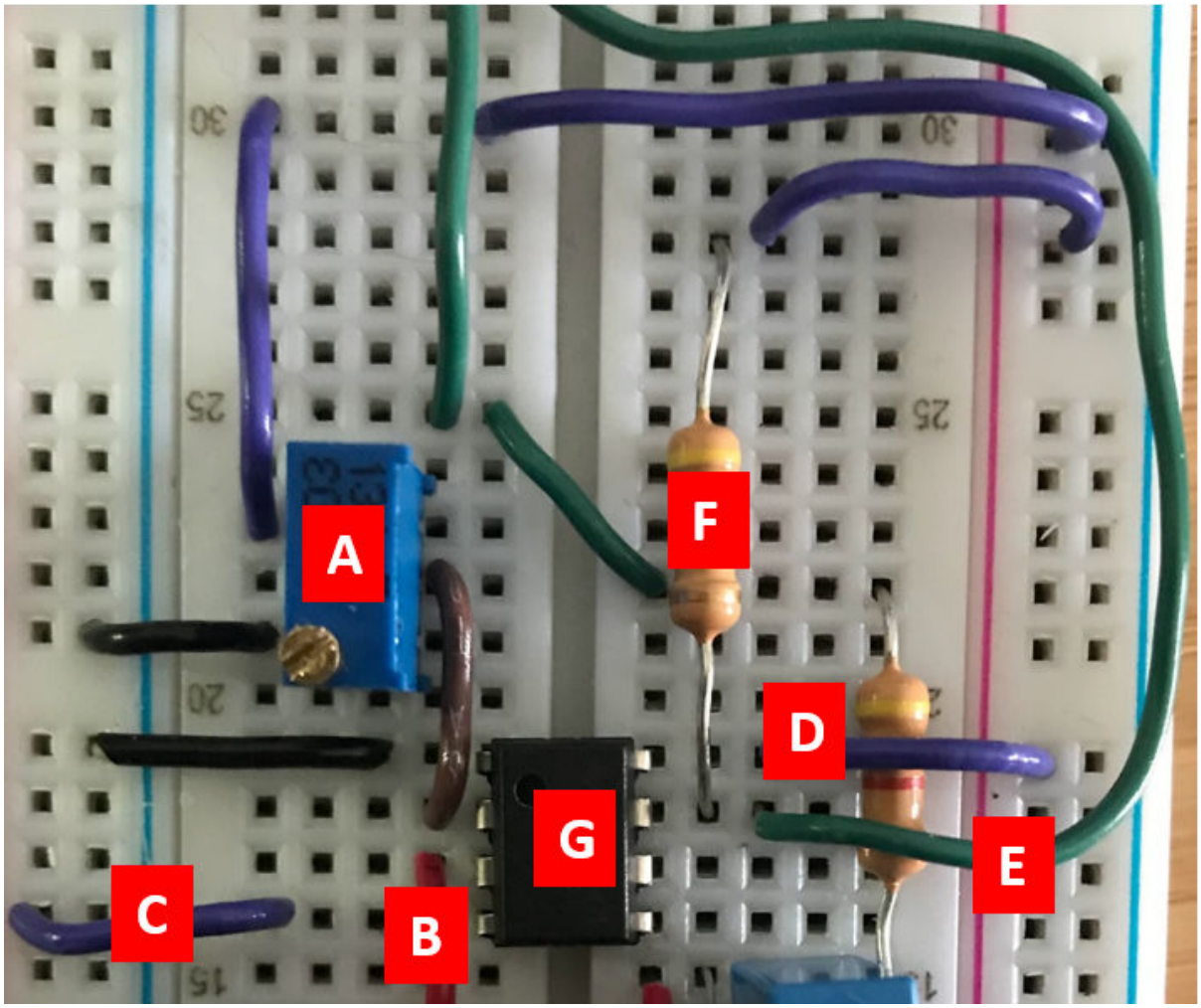


Figure 26: Constructed Comparator Circuit

A: 10 kΩ Potentiometer

B: Voltage ramp input

C: Ground

D: V_cc of 5V

E: Output of Comparator, used in later sections of the lab

F: 4.7 kΩ resistor

In the circuit, we connect the 5V Voltage input to the middle pin of the potentiometer, while 5V votlage supply is connected to the rear pin. This allows us to vary the voltage input at the negative terminal, as varying the resistance between these two pins will result in varying voltage by Ohms Law, $V = I * R$. At higher resistance between the two pins, we expect a higher voltage and vice versa. We use our voltage ramp from the previous section as an input, and connect the Input voltage as Channel 1 (Yellow Line) of the oscilloscope window below. Channel 2 (Blue line) shows the Voltage ramp input, while the logic analyzer window (bottom of screenshot) shows the output of the chip. As we can seem, once the voltage ramp exceeds the input voltage through the

potentiometer, the chip outputs to low as expected. It remains at this low output until the voltage ramp drops below the Voltage input level.

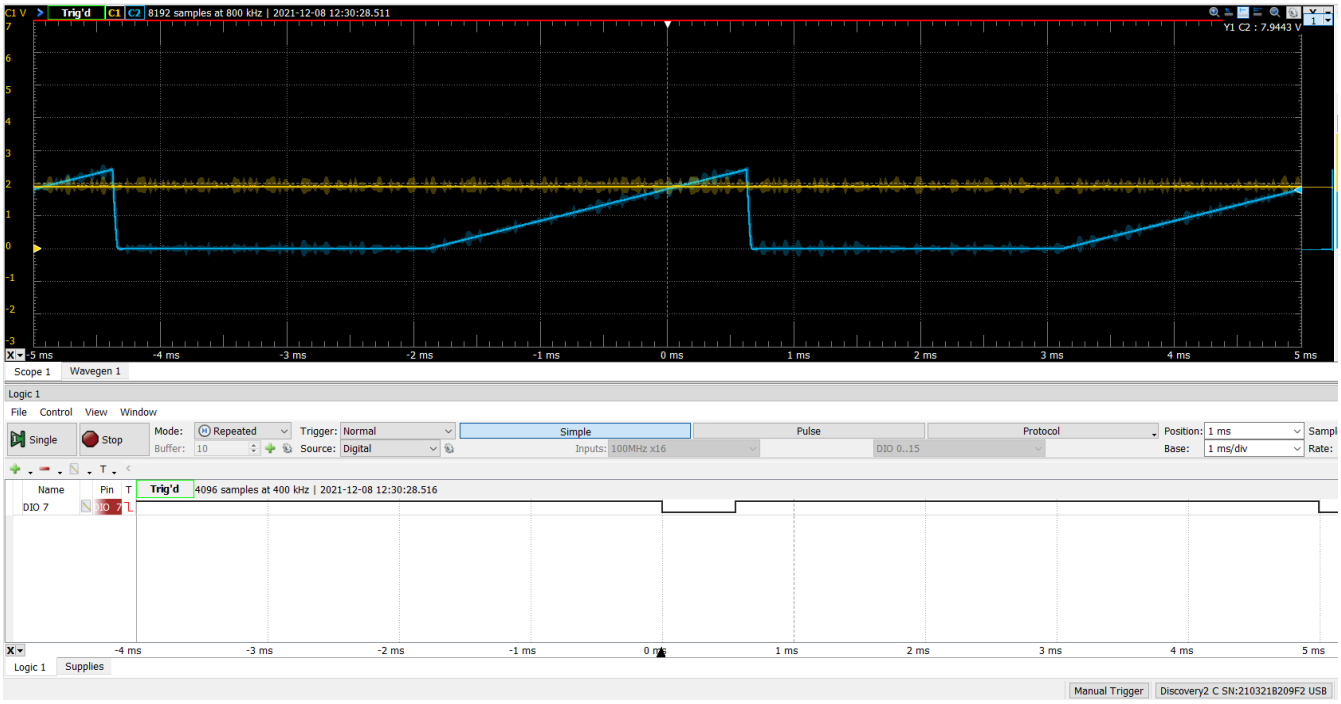


Figure 27: Voltage Ramp Input to Comparator with Input Voltage shown

I also observed that past a certain input voltage, the comparator is no longer able to drop to 0, even when the voltage ramp input has exceeded the input voltage. I tested where this occured by inputting a voltage ramp that was reached the 4.2V maximum found in the previous section, then varying the input voltage (by varying the resistance across the potentiometer terminals being used) unil I could no longer see the output dropping to low. This occured at an input voltage of approximately $3.9734 \pm V$. This is simply a feature of the chip, known as the saturation voltage and we expect this to vary based on the supply voltage provided. I was unable to find the expected value for this voltage on the datasheet of the chip.

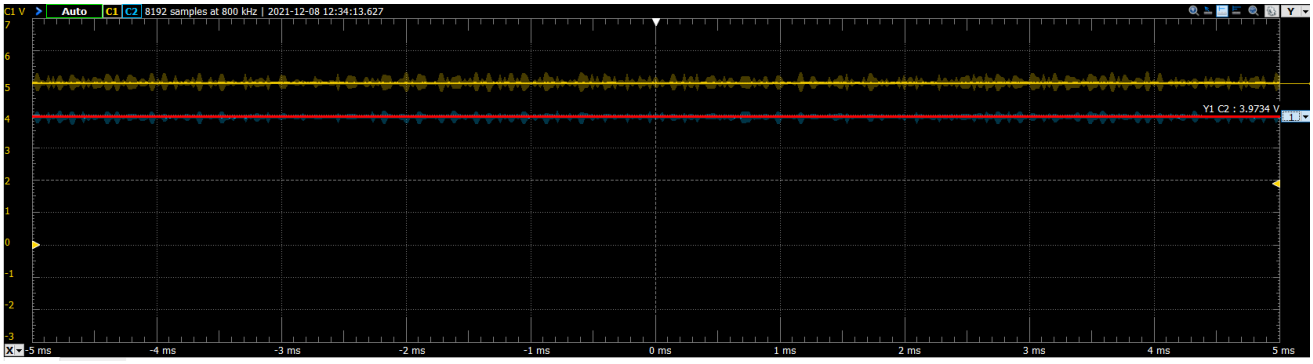


Figure 28: Saturation Voltage of Comparator Chip

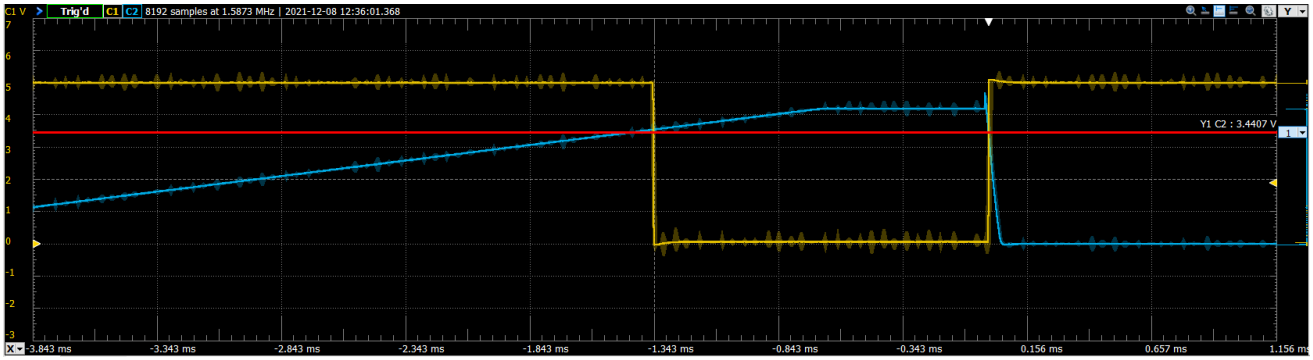


Figure 29: Behaviour of Comaprator

In the screenshot above, we simply input a voltage ramp and view the output of the comparator (Yellow Channel 1 Line) dropping to 0 once the input voltage (Indicated by the red cursor at 3.4497 V) has been exceeded by the Voltage ramp. Once again, this confirms the expected behaviour of the comparator.

As can be seen, the circuit functions as expected. By varying resistance across the 2 terminals of the potentiometer connected to the comparator, I am able to vary the input voltage. This allows me to vary the time at which an input voltage ramp exceeds the input voltage level, which is where the output of the comparator will drop to Lo. We are limited in the maximum level of voltage that can be compared to $3.9 \pm V$ due to the saturation voltage of the comparator.

3.5 Control Logic

In this section, we construct a flip flop using 2 NAND Gates. NAND Gates are logic gates with the following truth table.

```
InputA=['LO';'LO';'HI';'HI'];
InputB=['LO';'HI';'LO';'HI'];
Output=['HI';'HI';'HI';'LO'];
table(InputA,InputB,Output)
```

```
ans = 4×3 table
```

	InputA	InputB	Output
1	LO	LO	HI
2	LO	HI	HI
3	HI	LO	HI
4	HI	HI	LO

In order to construct the flip flop, we connect 2 NAND Gates as follows:

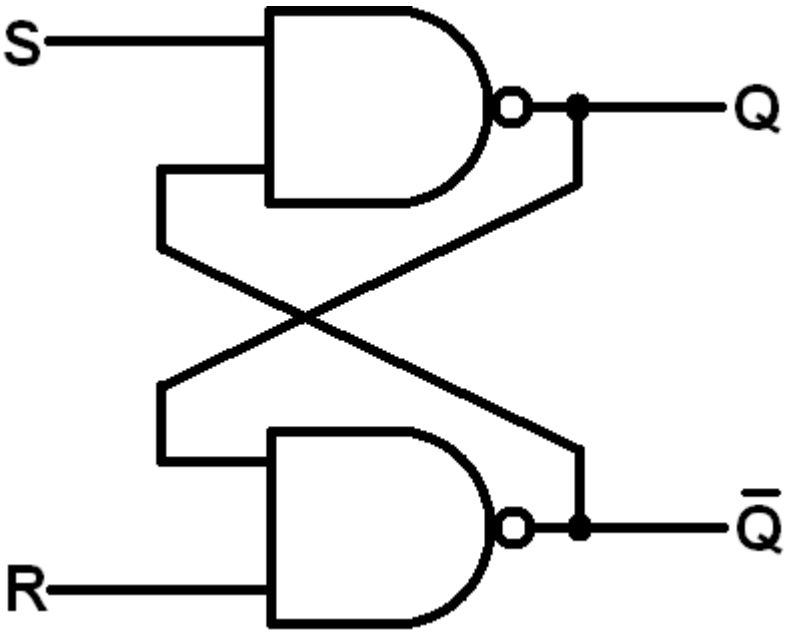


Figure 30: NAND Gate Diagram.

We try various combinations of HI and LO at the different terminals to see which ones are valid states. This results in a truth table as follows:

```
S=['HI';'HI';'LO';'HI'];
R=['LO';'HI';'HI';'HI'];
Q=['LO';'LO';'HI';'HI'];
Q_bar=['HI';'HI';'LO';'LO'];
table(S,R,Q,Q_bar)
```

ans = 4×4 table

	S	R	Q	Q_bar
1	HI	LO	LO	HI
2	HI	HI	LO	HI
3	LO	HI	HI	LO
4	HI	HI	HI	LO

As we can see, there are 2 valid states where S and R are both at HI. This allows the FlipFlop to act as a sort of memory based on the previous inputs at these terminals. If the input at S and R are LO and HI respectively, and S then switches to HI, we get a HI ouput at Q and a low output at Q_bar. If S and R start at HI and LO respectively and then R switches to HI, we get a LO ouput at Q and a HI output at Q_bar. Basically, when in the S and R are both HI, the outputs of Q and Q_bar are the same as their previous state (given that S and R were previously at opposite states).

Constructed Circuit

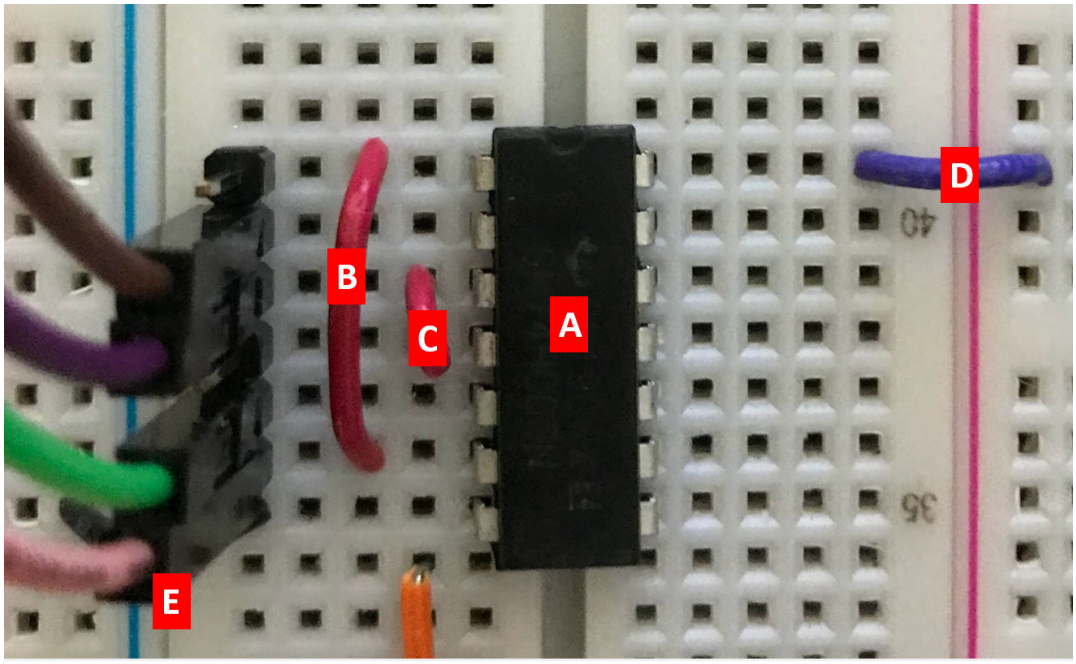


Figure 31: Constructed Flip Flop

A: NAND Gate Chip

B: Connection from Q_bar to input of NAND Gate 1 from circuit diagram.

C: Connection from Q to input of NAND Gate 2 from circuit Diagram

D: V_cc input of 5V

E: Ground

In order to test the functionality of the Flip-Flop, I used the logic analyzer and patterns program of my AD2, they are both seen below:

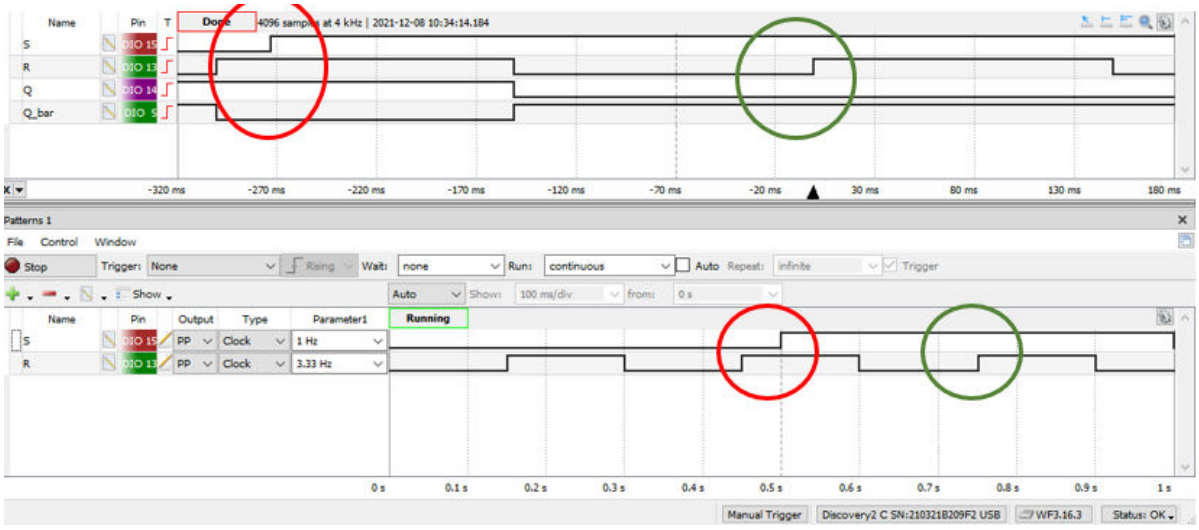


Figure 32: Logic Analyzer and Patterns App to test and confirm the Flip Flop

The patterns app (lower window) allows me to input pulses of different frequency at S and R pins, allowing me to see the ouputs for the various possible input combinations. The LO at S, HI at R to HI at both transition input can be seen circled in red, while the HI at S, LO at R to HI at both transition is seen circled in Green. As can be seen, the states of LO at S and HI at R But when S and R start with LO and HI respectively and transition to HI and HI, we get an ouptut of of HI at Q and LO and Q_bar. As explained above, this allows the FlipFlop to act as a type of memory as its output can be stores when both inputs are at HI, given that the inputs were previously at opposite states to each other. The outputs seen in the logic analyzer window above also show some undefined states, such as LO and LO inputs resulting in HI and HI, however these are not defined by the rules of the NAND gates used.

4. Integration of Components into an ADC

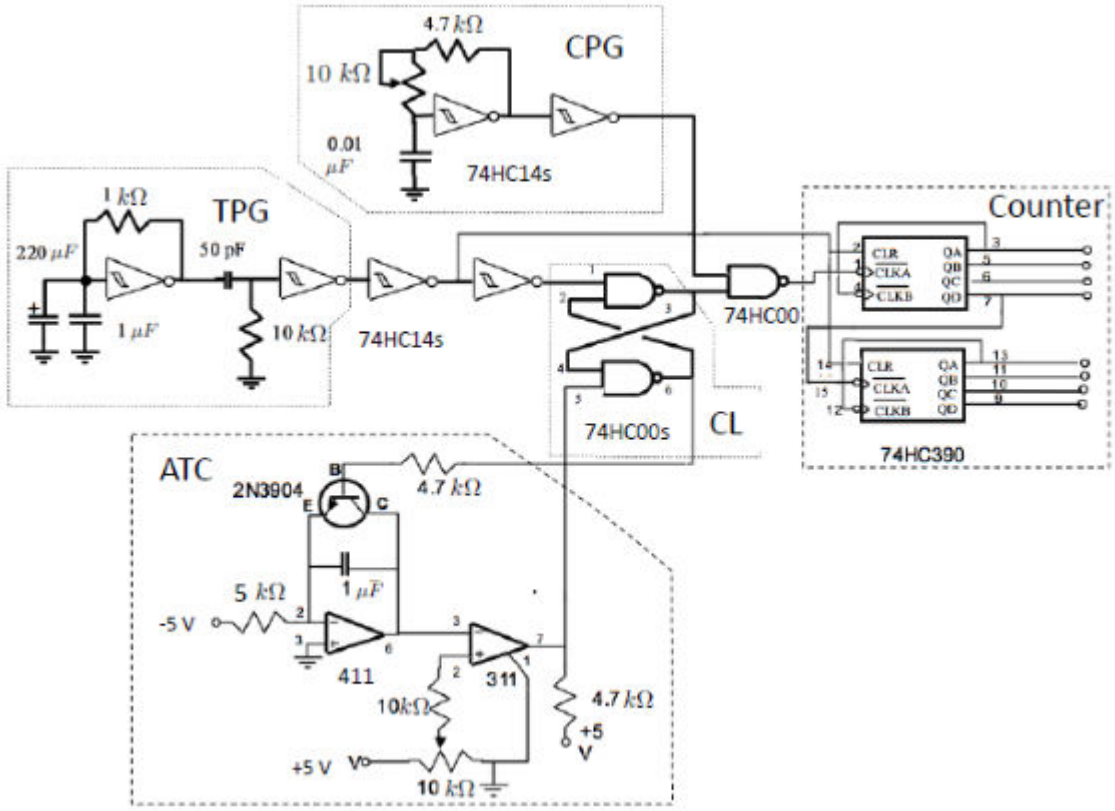


Figure 33: Final Circuit

The final part of this lab is to connect the variouis elements of the circuit above that we have explored above to create an analog to digital converter. In this circuit, the output of the TPG connects directly to the reset of our counter chip after going through one more Schmitt trigger. This means each pulse will reset the counter back to 0, based on the behaviour of the reset of the counter that we saw Section 3.3. The TPG also goes through one more inverter, returning it to being a short pulse from 5V to 0V. This goes to the set pin of our FlipFlop, which results in a LO input to one of the pins of a NAND gate to HI. This allows the CPG that is also connected to this NAND gate to create pulses at the Output of the NAND gate, as long as the the input from the FlipFlop to the NAND is HI. This is because when one pin of the NAND is HI, the other input can switch from LO to HI to cause the ouput to switch from HI to Lo. The clock pulses allow the counter to increment with each falling edge (HI to

LO transition). The two triggers between the initial TPG output allows for the clear signal to reach the counter before clock pulses can arrive due to the slight delay that it creates

The TPG input to the FlipFlop also results in a LO output to the transistor of our ATC, which allows for the integrator to function, as described in Section 3.4.1. This creates a HI output at the comparator until the input voltage of the comparator is exceeded, at which point, the output of the comaparator goes to LO .

In order to ensure that the number displayed by the digital display matches the input voltage at the ATC, we can vary the potentiometer at the CPG so that the number of pulses within the time window for which the NAND gate is open matches the input voltage. This simply requires measuring the input voltage, and varying the resistance accordingly. If the voltage displayed is lower than the input, we need more pulses to arrive at the counter within the time window, so we aim to increase the clock pulse frequency, which we can achieve by decreaseing the resistance at the potentiometer, according to section 3.2.

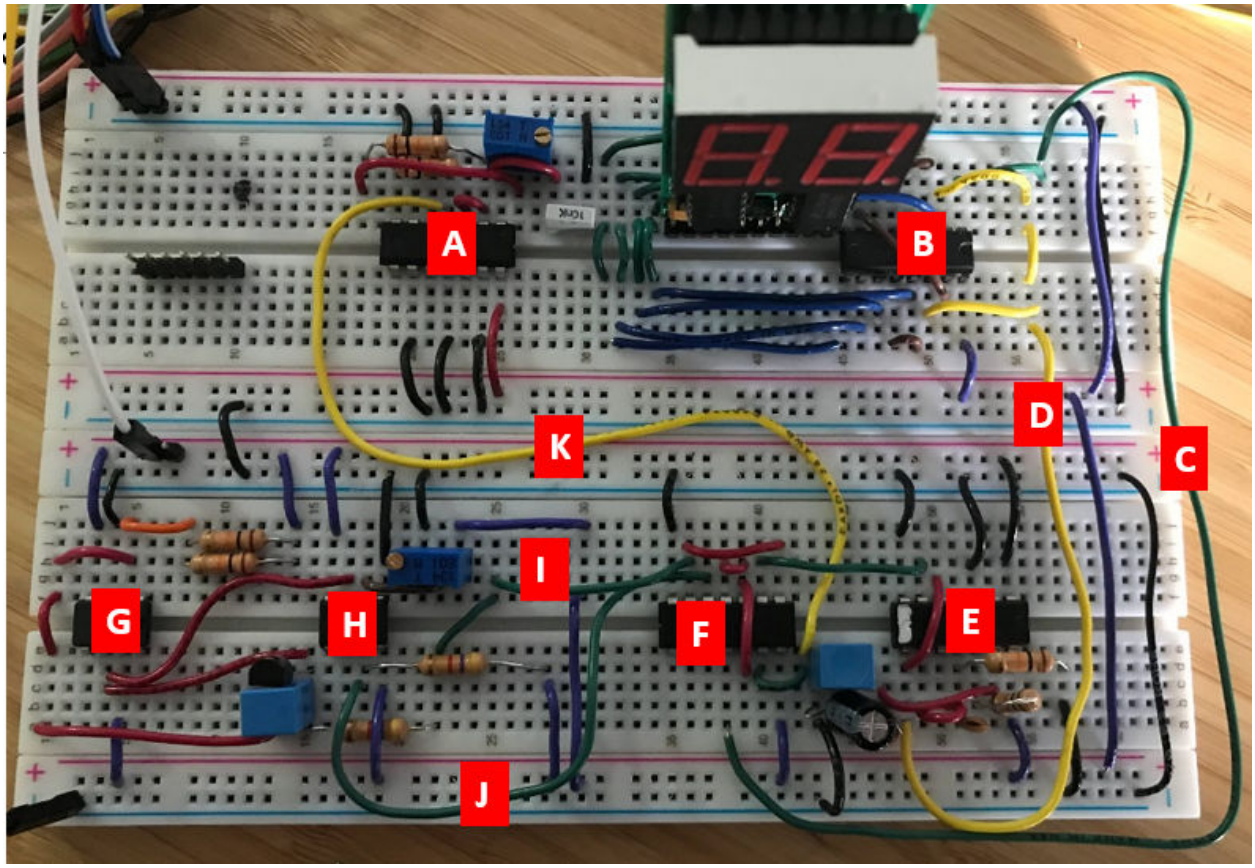


Figure 34: Constructed Final Circuit

A: Clock Pulse Generator

B: Counter

C: Logic Gate Output (Clock Pulse when open)

D: Trigger Pulse Generator to Counter Reset

E: Trigger Pulse Generator

F: FlipFlop

G: Integrator (Voltage Ramp Generator)

H: Comparator

I: Integrator Input

J: Comparator Output to FlipFlop

K: Clock Pulse Generator Output to Logic Gate

After constructing the circuit above, Voltage supplies were turned on, and the circuit was callibrated by adjusting the resistance of the clock pulse generator so that the number of clock pulses over a time window would match the voltage input. This could be done theoretically, by calculating the required frequency of the Clock pulse input and the resistance required for this, but due to the relative ease of simply adjusting the potentiometer, calculations were not done. In order to confirm that the voltage displayed was because the circuit was working as expected, we connect the oscilloscope to the Voltage Ramp Integrator and the Comparator outputs, as well as logic pins to the Clock Pulse Generator (output through the logic gates, so only pulses that reach the counter), Trigger Pulse Generator and Time Window (duration for which the input to the base of the transistor of the Integrator is 0). This generated the following:

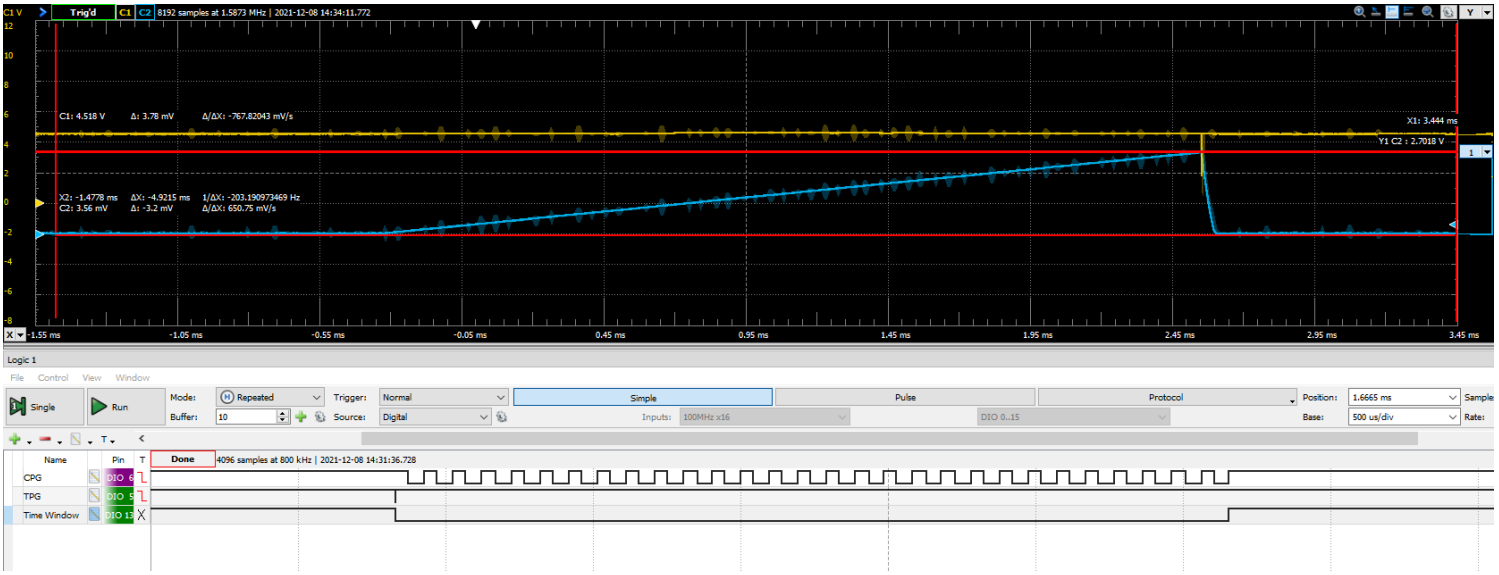


Figure 35: Timing Diagram showing Voltage or Logic State of Various Components from the constructed ciruit.

The diagram above shows the measure output for the various elements of the circuit over 1 iteration of counting to the input voltage. The blue line shown in the oscilloscope screen (top window in screenshot) shows the voltage ramp generator, growing until it reaches the input voltage of 2.7 V. At this point, the comparator of the ATC transitions to LO. This is seen with the yellow line in the osciloscope screen. While the ramp is rising to the input voltage, we can look at the logic analyzer and view the clock pulse generator pulses that reach the counter while the gate is open. We count and see that there are 27 falling edges within the time window, resulting in the displayed 27 on the digital display. We also see the initial TPG pulse which opens the gate for the CPG to reach the counter and for the integrator to begin it's ramp. Finally,see the TIme Window in the logic analyze which measures the output at the Q_bar terminal fo the FlipFlop, which is low for the duration of the counting. This terminal is connected to the transistor of the Integrator of the ATC, which must be LO so that the capacitor is not

shorted, and the integration can occur. This repeats as a cycle with each TPG pulse resetting the counter and initiating the voltage ramp again. The cycle happens rapidly, as we can see above, with a short time window of less than 3 ms, which is why the display flickers when it is showing the volltage, as it is rapidly counting to the voltage, resetting, then counting again.

As we vary the voltage input, the integrator is able to reach the input voltage level faster, since it has a constant slope, as we found earlier. This means fewer clock pulses will be counted within the time window and the voltage displayed will be lower. By callibrating our circuit, we are able to achieve the correct voltage displayed for teh range of voltage inputs.

5. Troubleshooting

I initially struggled with the variable resistor as understanding which terminals to connect caused some level of confusion. This meant that my intial attempts to set up the circuit for section 3.2 were unsuccessful. After a few attempts, I took the variable resistor out and began measuring the resistance across the terminals to figure out how exactly they worked. Once I was able to build a model in my mind, it became easy to setup the circuit. I then reconnected the resistor and was able to get the square pulse generator running fairly quickly.

I also initially had issues during my first attempt to measure the hysterisis of the chip, but upon verifying my connections and transferring to a different trigger, I realized that one of my triggers did not work and was simply faulty. During the course of the lab, I often had issues with the Schmitt Trigger. Upon testing my final circuit for the first time, when I went to turn it on, I found that the circuit did not work and used my oscilloscope to analyze where I was getting unexpected readings and found that my TPG was not outputting any pulses. I began checking the wiring and tested the various parts, measuring resistances and capacitances along the way, but was not able to find any issues. I then switched Schmitt Trigger chips and was able to get the necessary output again. I then had trouble with my CPG which had a flat input and output. While troubleshooting this, I was told that the chips may have issues when all of their terminals are in use, due to some interference between the channels. I then changed my wiring to use 2 Schmitt Triggers, one for the CPG portion of the circuit and one for the TPG.

Upon further testing of my circuit, I found that it's behaviour was changing when I touched or moved certain wires, which lead me to believe there may be connection issues in areas of the circuit. I carefully checked my connections and found that some of my wiring was not well inserted, which meant they were susceptible to being pulled out or disturbed in other ways. I rewired these sections, ensuring that wiring was inserted deep into the breadboard. There were also times where it seemed that connections within the breadboard may be faulty, so I used the continuity tester function of my DMM in order to ensure that this was not causing any problems.

6. Conclusion

This lab provided an incredible learning experience on analog to digital circuits. I was able to use the knowledge that I had accumulated over the course of the term, on transistors, Op Amps, Capacitors and logic gates towards building this exciting circuit. I now clearly understand some of the concepts better, and can see myself applying these towards designing circuits in the future. This circuit also rpovided a valuable opportunity to develop my troubleshooting skills, as there were range of issues that I faced during the process.